LQD-M85400-SR4C

400G QSFP-DD SR4 MPO-12/APC Transceiver

Product Features

- 8x50G PAM4 retimed 400GAUI-8 electrical interface
- MPO-12 APC connector
- 4 channel VCSEL arrays and 4 channels PIN photo detector arrays
- Maximum link length of 30m on OM3 or 50m on OM4
- Compliant to QSFP-DD Module Specification Rev 6.0
- Compliant with CMIS 5.2
- Compliant with IEEE 802.3db
- Compliant to IEEE 802.3bs
- Less than 8W in temperature range of 0 to 70℃

Applications

- Data centers and Cloud Networks
- 400GE Interconnect Requirements.

Standards

- IEEE 802.3cd
- QSFP-DD MSA
- CMIS 5.2

Description

The LINK-PP LQD-M85400-SR4C is a four-Channel, Parallel, Pluggable, Fiber-Optic QSFP-DD Module for 400Gigabit Ethernet applications. This product converts 8 channels of 26.5625GBd electrical input data to 4 channels of 53.125GBd parallel optical signals. Reversely, on the receiver side, 4 channels of parallel optical signals of 53.125GBd converts to 8 channels of 26.5625GBd electrical output data. This module is designed to operate over multimode fiber systems using a nominal wavelength of 850nm, up to 30 meters over OM3 MMF or 500 meters over OM4 MMF.

Absolute Maximum Ratings

Product	Electrical mode	Protocol	Nominal Rate			Specifications	
			Aggregate (Gbps)	Electrical Lanes(Gbaud)	ppm	High Speed Electrical	Pre-FEC Max BER
400G-SR4	8X50	IEEE802.3cd	425	26.5625 PAM4	±100	400GAUI-8	2.4E-4

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-40	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	RH	0	85	%

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tca	ºC	0	/	70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Power Consumption	Pc	W		7.5	8

Transmitter characteristics

Parameter		Symbol	Min	Typical	Max	Unit
Optic Data rate per lane		DR		53.125		GBd
Modulation format				PAM4		
Center Wavelength [1]		λ	840	860	868	nm
RMS spectral width		σ			0.6	nm
Average Launch power, each lane		P_{avg}	-4.6		4	dBm
Optical Power OMA, each Lane, max		P_{OMA}		3.5		dBm
OMAouter, each lane min	max (TECQ, TDECQ) <1.8 dB			max [-2.6 , max(TECQ,TECQ) – 4.4]		dBm
	1.8 < max (TECQ, TDECQ) < 4.4 dB					
Transmitter and dispersion eye closure (TDECQ), each lane		TDECQ			4.4	dB
Transmitter eye closure for PAM4 (TECQ), each lane		TECQ			4.4	dB

Extinction ratio	ER	2.5			dB
Transmitter power excursion, each lane				2.3	dBm
Optical Return Loss Tolerance	ORLT			14	dB
Optical Power for TX DISABLE				-30	dBm
Encircled fluxb[2]		⩾86% at 19 um ⩽30% at 4.5 um			

Notes:

1. Defined according to the performance of the laser used.
2. Measured into type A1a.2 or type A1a.3, or A1a.4, 50 um fiber, in accordance with IEC 61280-1-4

Receiver characteristics

Parameter		Symbol	Min	Typical	Max	Unit
Data rate per lane		BR		53.125		Gbd
Modulation format			PAM4			
Center Wavelength		λ	842	850	948	nm
Damage threshold			5			dBm
Average receive power, each lane			－6.4		4	dBm
Receive power, each lane (OMAouter)					3.5	dBm
Receiver reflectance		Rr			－15	dB
Receiver sensitivity(OMA), each lane[1]			RS = max (-4.6 , TECQ － 6.4)			dBm
Stressed receiver sensitivity, each lane					－2	dBm
Rx LOS	Assert		-15			dBm
	De-assert				-7.5	dBm
	Hysteresis		0.5		5	dB

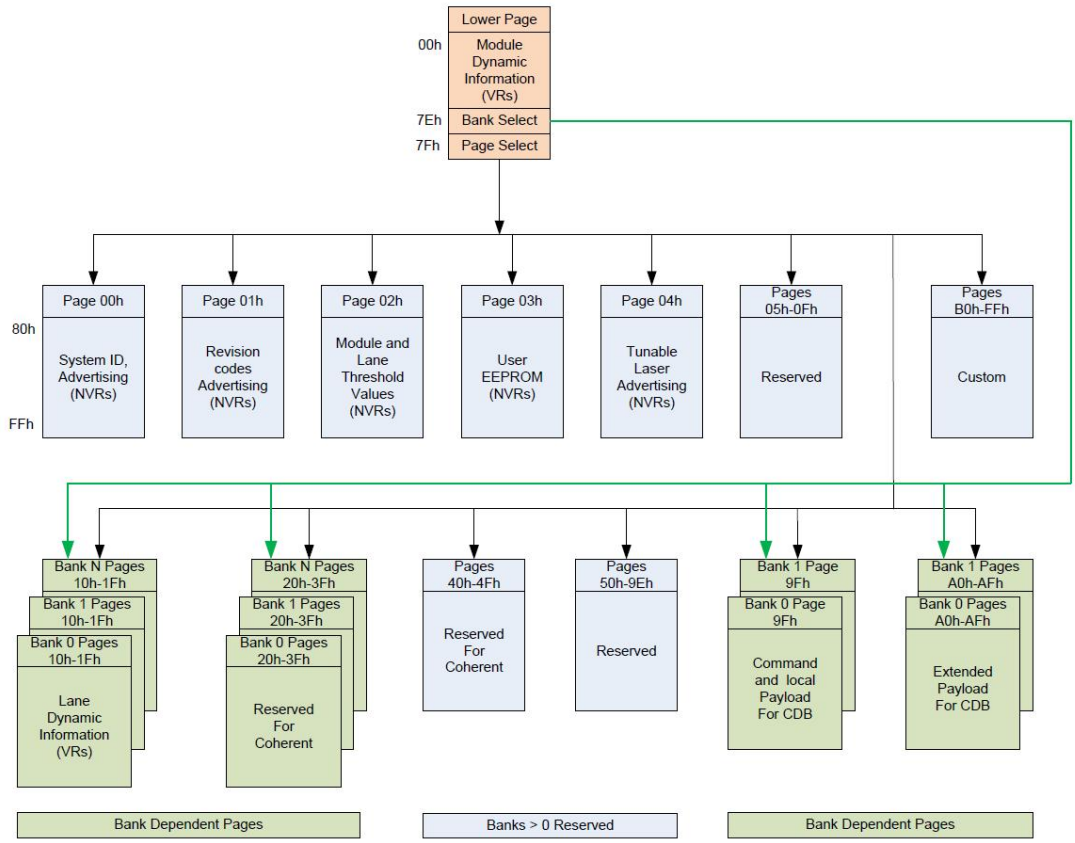
Notes:

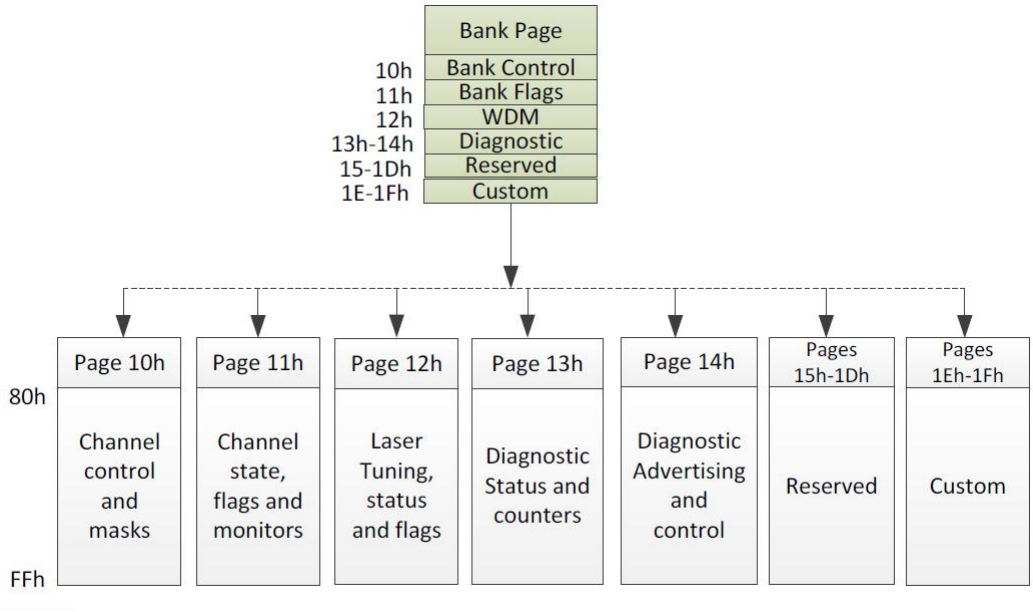
3. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

Electrical Specification

Parameters	Min	Typical	Max	Unit
Supply Voltage	3.135		3.465	V
Input Differential Impedance	90	100	110	Ω
Differential data input swing			880	mVpp
Differential data output swing			900	mVpp
Bit Error Rate			2.4E-4	
Input Logic Level High	2		v_{cc}	v
Input Logic Level Low	0		0.8	v
Output Logic Level High	V_{cc}-0.5		v_{cc}	v
Output Logic Level Low	0		0.4	v

Management Interface





CMIS Module Memory Map

Multiple Applications Support

The module supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

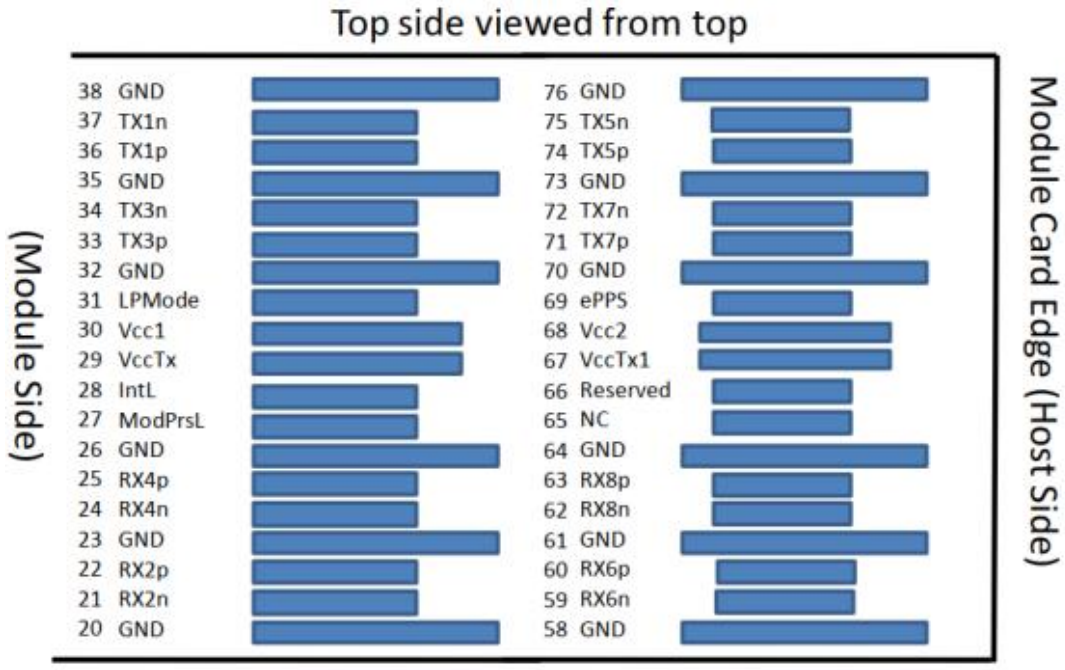
Application Advertising

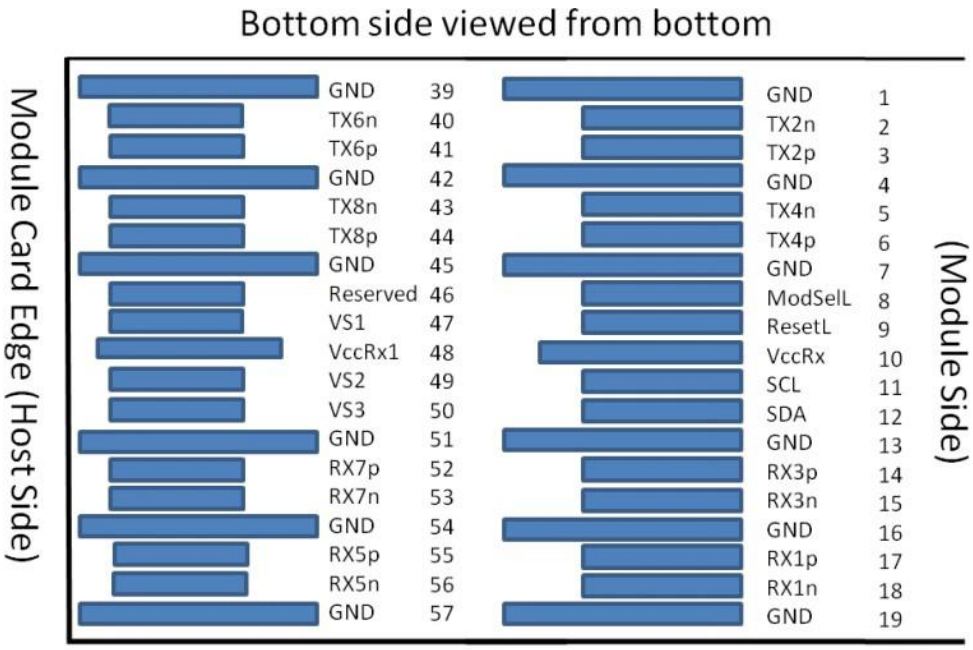
Address (Dec)	Application		Value (Hex)	Description
	AppSel Code	Name		
85	NA	Module Type encoding	1	Optical Interfaces: MMF
86	0001b	HostInterfaceID	31	HostInterfaceIDApp1: IB HDR
87		MediaInterfaceID	11	MediaInterfaceIDApp1: 400G-SR4
88		HostLaneCount&MediaLaneCount	84	LaneCountApp1: host 8 lanes, media 4 lanes
89		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:176		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
90	0010b	HostInterfaceID	11	HostInterfaceIDApp2:400GAUI-8 C2M
91		MediaInterfaceID	11	MediaInterfaceIDApp2: 400G-SR4
92		HostLaneCount&MediaLaneCount	84	LaneCountApp2: host 8 lanes, media 4 lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:177		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
94	0011b	HostInterfaceID	F	HostInterfaceIDApp3:200GAUI-4
95		MediaInterfaceID	1B	MediaInterfaceIDApp3:200GBASE-SR2

96		HostLaneCount&MediaLaneCount	42	LaneCountApp3:host 4 lanes, media 2 lanes
97		HostLaneAssignmentOptions	11	Permissible first host lane number: lane 1，5
01h:178		MediaLaneAssignmentOptions	5	Permissible first media lane numbern: lane 1,3
98	0100b	HostInterfaceID	D	HostInterfaceIDApp4: 100GAUI-2 C2M
99		MediaInterfaceID	D	MediaInterfaceIDApp4:100GBASE-SR1
100		HostLaneCount&MediaLaneCount	21	LaneCountApp4：host 2 lanes, media 1 lanes
101		HostLaneAssignmentOptions	55	Permissible first host lane number: lanes 1, 3，5，7
01h:179		MediaLaneAssignmentOptions	F	Permissible first media lane number: lanes 1, 2, 3, 4
102	0101b	HostInterfaceID	FF	HostInterfaceIDApp5
103		MediaInterfaceID	0	MediaInterfaceIDApp5
104		HostLaneCount&MediaLaneCount	0	LaneCountApp5
105		HostLaneAssignmentOptions	0	HostLaneAssignmentOptionsApp5

As shown in the table above，the module supports 4 applications, IB HDR 400GBASE-SR4 and Ethernet 400GBASE-SR4,200GBASE-SR2,100GBASE-SR1.

Pin Description





Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3		Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModselL	Module select	3B	
9	LVTTL-I	Resetl	Module Reset	3B	
10		VccRx	+3.3V Power supply Receiver	2B	2
11	LVCMOSI/0	SCL	2-wire serial interface clock	3B	
12	LVCMOSI/0	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	
14	CML-0	Rx3P	Receiver Non-Inverted Data output	3B	1
15	CML-0	Rx3n	Receiver Inverted Data utput	3B	
16		GND		1B	1
17	CML-0	Rx1p	Receiver Non-Inverted Data output	3B	
18	CML-0	Rxln	Receiver Inverted Data output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-0	Rx2n	Receiver Inverted Data output	3B	

22	CML-0	Rx2p	Receiver Non-Inverted Data output	3B	
23		GND	Ground	1B	1
24	CML-0	Rx4n	Receiver Inverted Data output	3B	
25	CML-0	Rx4p	Receiver Non-Inverted Data output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	Intl	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	1
30		Vcc1	+3.3V Power supply	2B	1
31	LVTTL-I	LPMode	Low Power mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1P	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Txln	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbo1	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6P	Transmitter Non-Inverted Data Input	3A	1
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		Vs1	Module Vendor specific 1	3A	3
48		VccRx1	3.3v Power supply	2A	2
49		Vs2	Module Vendor specific 2	3A	3
50		Vs3	Module Vendor specific 3	3A	3
51		GND	Ground	1A	1
52	CML-0	Rx7P	Transmitter Non-Inverted Data Input	3A	
53	CML-0	Rx7n	Receiver Inverted Data output	3A	
54		GND	Ground	1A	1
55	CML-0	Rx5p	Transmitter Non-Inverted Data Input	3A	
56	CML-0	Rx5n	Receiver Inverted Data utput	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-0	Rx6n	Transmitter Inverted Data Input	3A	
60	CML-0	Rx6p	Transmitter Non-Inverted Data Input	3A	
61		GND	Ground	1A	1
62	CML-0	Rx8n	Transmitter Inverted Data Input	3A	

63	CML-0	Rx8p	Transmitter Non-Inverted Data Input	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1		2A	2
68		Vcc2		2A	2
69		ePPs		3A	3
70		GND	Ground	1A	1
71		Tx7P	Transmitter Non-Inverted Data Input	3A	
72		Tx7n		3A	
73		GND	Ground	1A	1
74		Tx5p	Transmitter Non-Inverted Data Input	3A	
75		Tx5n		3A	
76		GND	Ground	1A	1

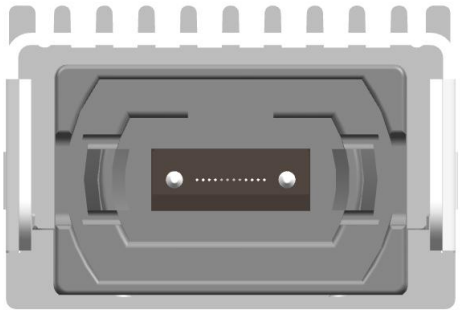
Note 1: QSFP-DD uses comon ground (GND)for all signals and supply (power). A11 are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted, connect these directly to the host board signal-common ground plane .

Note 2: VccRx,VccRx1,Vccl, Vcc2, VccTx and VccTxl shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx,VccRxl, Vccl, Vcc2, VccTx and vccTxl may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor specific, Reserved, No connect and ePPs (if not used) pins may be terminated with 50 ohms to ground on the host, Pad 65 (No Connect) shall be left unconnected within the module.Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

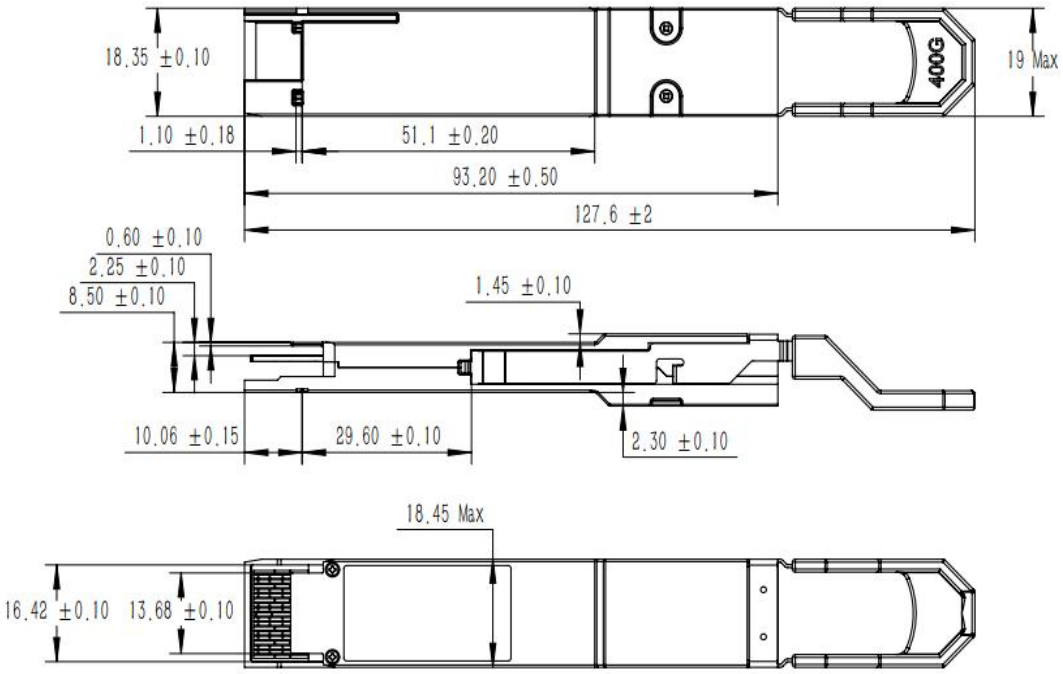
Note 4: Plug Sequence specifies the mating sequence of the host connector and module, The sequence is 1A, 2A, 3A, 1B, 2B, 3B, (see Figure 2 for pad locations)Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B,followed by 3A, 3B

Optical interface



Package Outline

Compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.



Ordering information

Part Number	Product Description
LQD-M85400-SR4C	MPO-12/APC, 850nm, 400Gbps, QSFP-DD, SR4, 50m, 0° C~+70°C, with DDM