LQD-M31400-LR4C

400G-PLR4 QSFPDD 1310nm 10km MTP/MPO Transceiver for SMF

Product Features

- Maximum Power Consumption 9W
- Case Operating Temperature 0˚C to 70˚C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser
- Compliant with QSFP-DD MSA HW Rev 5.0 Type 2 Housing with MPO-12 Connector
- Compliant with QSFP-DD CMIS Rev 5.0
- Compliant with EU Directive 2011/65/EU (RoHS Compliant)
- Compliant with IEEE802.3bs Standard: 400GAUI-8 Electrical Interface
- Compliant with IEEE802.3cu Standard: 4x100GBASE-LR1 Optical Interface

Applications

- 400G Ethernet
- Data Center Interconnect
- Infiniband Interconnect
- Enterprise Networking

Description

LQD-M31400-LR4C is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 10km optical communication applications. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi- Source Agreement (MSA).

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature Range	Ts	-40	85	℃	
Relative Humidity (Non-condensing)	RH	5	95	%	
Supply Voltage	VCC	-0.5	3.6	V	
Control Input Voltage	VI	-0.3	VCC+0.5	V	

Recommended Operating Conditions

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Operating Case Temperature	TOPR	0		70	℃	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	ICC_IP			4000	mA	
Sustained Peak Current at Hot Plug	ICC_SP			3300	mA	
Maximum Power Dissipation	PD			10	W	
Maximum Power Dissipation, Low Power Mode	PDLP			1.5	W	
Signalling Rate Per Lane	SRL		53.125		GBd	PAM4
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise Tolerance (10Hz-10MHz)				66	mV	
Rx Differential Data Output Load			100		Ohm	
Operating Distance		2		10000	m	

Electrical Characteristics Low Speed Signal

Parameter	Symbol	Min	Max	Unit	Notes
Module Output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
		-0.3	0.8		

Parameter	Symbol	Min	Max	Unit	Notes
InitMode, ResetL and ModSelL	VIL			V	
	VIH	2	VCC+0.3	V	
IntL	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	

Electrical Characteristics High Speed Signal

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Wavelength	λC	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, Each Lane	AOPL	-1.9		4.8	dBm	1
Outer Optical Modulation Amplitude (OMAouter), Each Lane	TOMA			5	dBm	
Outer Optical Modulation Amplitude (OMAouter), Each Lane: for TDECQ <1.4dB for 1.4≤TDECQ≤3.4dB	TOMA	1.1 -0.3+TDECQ			dBm	
Transmitter and Dispersion Eye Closure for PAM4(TDECQ), Each Lane	TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4(TECQ)	TECQ			3.4	dB	
|TDECQ-TECQ|				2.5	dB	
Over/Under-shoot				22	%	
Transmitter Power Excursion				2.8	dBm	
Average Launch Power of OFF Transmitter, Each Lane	TOFF			-15	dBm	
ExtinctionRatio, Each Lane	ER	3.5			dB	
RIN15.6OMA	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.6	dB	
Transmitter Reflectance	TR			-26	dB	
Transmitter Transition Time	Tt			17	ps	
Receiver						
Wavelength	λC	1304.5	1311	1317.5	nm	
Damage Threshold, Each Lane	AOPD	5.8			dBm	
Average Receive Power, Each Lane	AOPR	-8.2		4.8	dBm	2
Receive Power(OMAouter), Each Lane	OMAR			5	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity(OMAouter), Each Lane	SOMA			-6.1	dBm	

Parameter	Symbol	Min	Typ	Max	Unit	Notes
for TECQ<1.4dB for1.4≤TECQ≤3.4dB				-7.5+TECQ		
Stressed Receiver Sensitivity(OMAouter), Each Lane	SRS			-4.1	dBm	3
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4(SECQ)			3.4		dB	

Notes:
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Average receive power, (min) is informative and not the principal indicator of signal strength.
3. Measured with conformance test signal at TP3 for the BER = 2.4x10-4.

QSFP-DD Edge Connector and Pinout Description

The electrical pinout of the QSFP-DD module is shown in Figure 1 below.

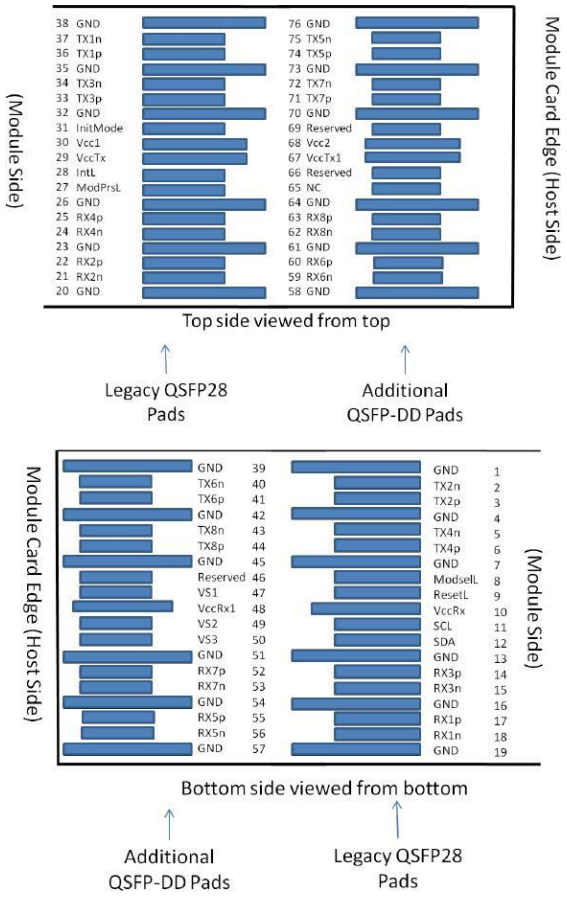


Figure 1. Host PCB QSFP-DD pad assignment top view

Pin No.	Symbol	Description	Note
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	Init Mode	Initialization mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Ground	1

Pin No.	Symbol	Description	Note
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data output	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data output	
45	GND	Ground	1
46	Reserved	For Future Use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3V power supply	2
68	Vcc2	3.3V power supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Output	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Output	
76	GND	Ground	1

Note:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane;

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card

Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA;

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10

kOhms and less than 100 pF;

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur

simultaneously, followed by 2A, 2B, followed by 3A,3B.

Module Block Diagram

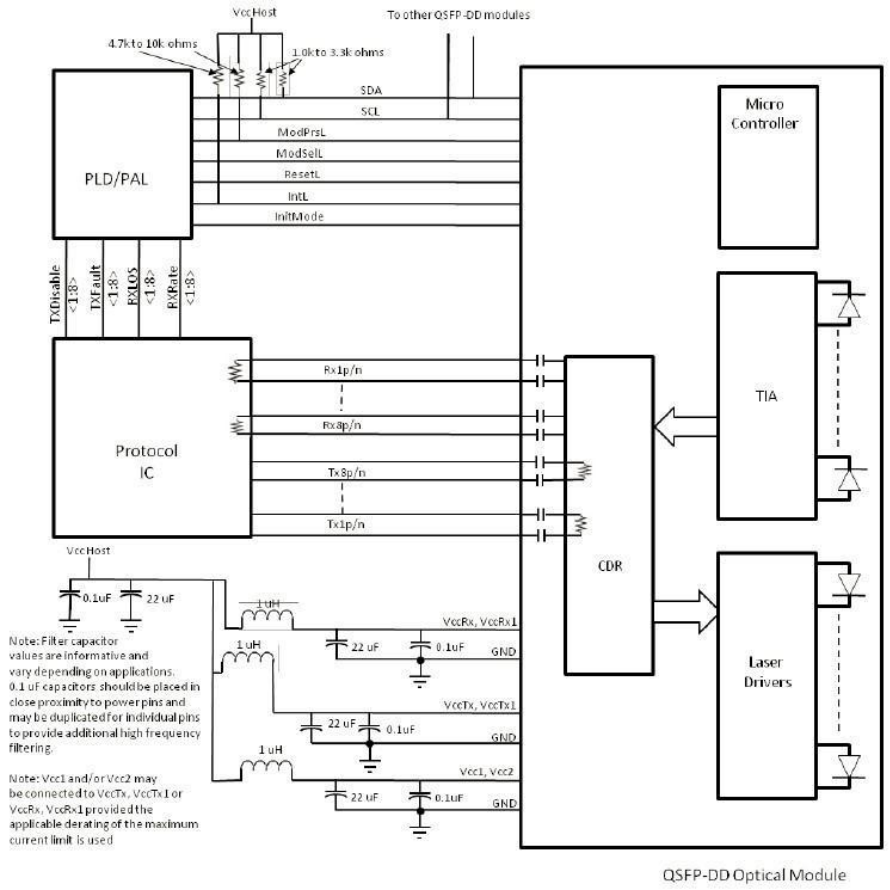
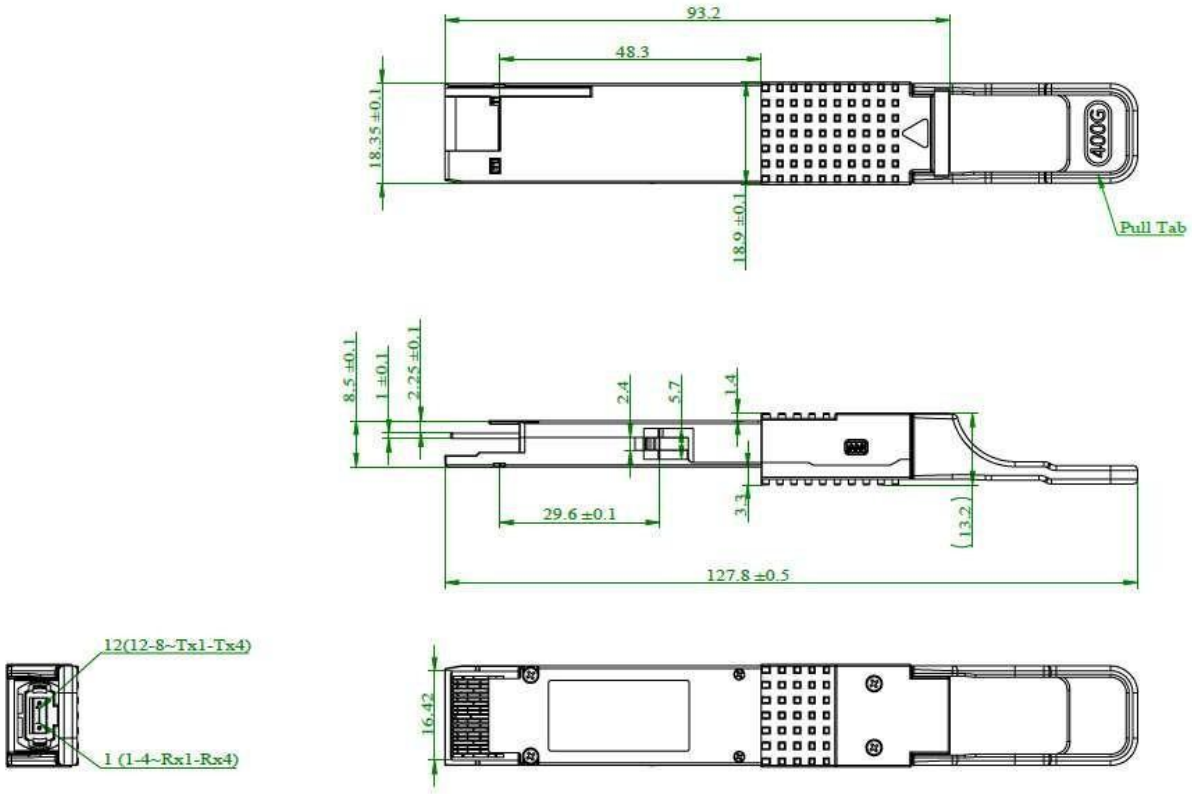


Figure 2. Module Block Diagram

Mechanical Specifications



Ordering information

Part Number	Product Description
LQD-M31400-LR4C	400Gbps, QSFP-DD, LR4, 10km, 0~+70° C, with DDM, MPO-12/APC connector