LQD-M31400-FR1SC

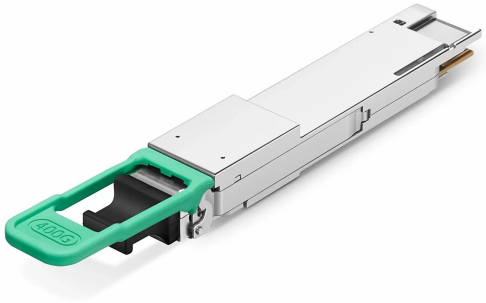
QSFP-DD 400GBASE-FR PAM4 1310nm
MPO-12/APC 2km Silicon Photonics Transceiver

Product Features

- QSFP-DD MSA compliant
- MPO-12/APC connector
- Power consumption <11 W
- Operating case temperature 0 to 70 ºC
- CMIS 4.0 management interface
- 4x 100GBASE-FR1 compliant 53.125GBd PAM4
- 100GAUI-2 compliant 2x 26.5625 GBd PAM4 Aggregation Mode
- 400GBASE-FR4 compliant 4x 53.125GBd PAM4
- 400GAUI-8 compliant 8x 26.5625 GBd PAM4

Applications

- Data Center 400GE 2km SMF links
- 400GE to 4 x100GE breakout over 2km
- Switch/Router interconnections



Description

The 4x 100G QSFP-DD FR1 optical transceiver that provides 4 parallel 100GE links over 4 single mode fiber (SMF) pairs via its MPO-12 connector. Each fiber pair link is compliant to 100GBASE-FR1 and thus can support a 400GE to 4x 100GE breakout over 2 km. It combines 8x 26.5625 GBd PAM4 electrical lanes into 4x 53.125 GBd PAM4 optical lanes. Superior performance and reliability is achieved through FS’s advanced integrated design using SiP engine (PIC with Quad MZM and PIN-Photo Diode, SMT Quad DRV and TIA), and Single cooled CW DFB Laser Sub-Module.

Functional Description

The 4x 100GBASE-FR1 is a fully integrated, 425 Gb/s optical transceiver for links up to 2 km by means PSM to the transmit and receive ports of the MPO-12 connector. In Breakout Mode, 4x 100GBASE-FR1 is complied with the optical interface specification IEEE Std 802.3-2022 Section 8 100GBASE-FR1 per lane. 100GBASE-FR1 specifies the use of PAM4 at 53.125 Gbaud operating at the channel with wavelength on the range of 1304.5-1317.5 nm from single cooled CW DFB-LD operated by quad MZM built in PIC via quad driver surfaced-mounted to PIC. The bit rate per lane is 106.25 Gb/s, which produces an aggregate data rate of 425 Gb/s by means PSM to the transmit ports of the MPO-12 connector. The received optical lanes are paralleled from the receive MPO-12 connector ports to quad PIN-PD built in PIC to recover the PAM4 for interfacing with the electrical interface via with quad transimpedance amplifier (TIA) surfaced- mounted to PIC as with quad driver.

The electrical interface is in compliance with 100GAUI-2 specified in IEEE Std 802.3-2022 Section 8. 100GAUI-2 specifies the use of two differential electrical lanes operating at 26.5625 GBd PAM4 per lane. The bit rate per lane is 53.125 Gb/s. 4x 100GBASE-FR1 has four sets of the two lanes specified by 100GAUI-2. By means of a 2: 1 mux/demux in DSP, 100GBASE-FR1 optical interface is connected to 100GAUI-2 electrical interface.

In addition, by selecting Aggregation Mode, 4x 100GBASE-FR1 transmits aggregated data rate of 425Gbps defined by IEEE Std 802.3-2022 Section 9. The aggregated data specifies the use of PAM4 at 53.125 Gbaud operating at four parallel channels. The bit rate per lane is 106.25 Gb/s, which produces an aggregate data rate of 425 Gb/s by means PSM to the transmit ports of the MPO-12 connector. The received optical lanes are paralleled from the receive MPO-12 connector ports to recover the PAM4 for interfacing with the electrical interface. 400GAUI-8 specifies the use of eight differential electrical lanes operating at 26.5625 GBd PAM4 per lane, and it is defined by IEEE Std 802.3-2022 Section 8. The bit rate per lane is 53.125 Gb/s, resulting in an aggregate data rate of 425 Gb/s that matches the optical line interface. An internal gear box in DSP converts between the eight lanes of the host interface and the four lanes of the line interface.

The bit error ratio (BER) of the optical interface is required by 100GBASE-R (Breakout Mode) and 400GBASE-R (Aggregation Mode) to be less than 2.4 x 10-4. The host side shall have Forward Error Correction (FEC) capability based on RS(544,514) requirements defined by IEEE Std 802.3-2022 Section 8 to meet the frame loss ratio requirements of 4x 100GE and 400GE.

The form factor of 4x 100GBASE-FR1 is QSFP56-DD Type 2A and is compliant with the hardware and Common Management Interface Specifications (MIS) of the QSFP-DD multi-source agreement (MSA). QSFP-DD modules

can support up to eight electrical lanes on the host interface, which is double the number of lanes supported by QSFP28 or QSFP+ modules. The unique feature of QSFP-DD ports is that they are mechanically and electrically compatible with QSFP28 and QSFP+. Hence, the same port can be used to support multiple generations of modules and data rates if the networking hardware is designed for such operation.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only.Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Unit	Min	Typ	Max	Note
Supply Voltage	Vcc	0		+3.6	V
Storage Temperature		-40		85	°C
Optical ReceiverInput				+5.0	dBm

Recommended Operating Conditions

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Voltage Noise Tolerance	PSNR			66	mV	10Hz–10MHz
Power Consumption	P_6			11	W	
Instantaneous Peak Current	Icc_ip_6			4400	mA	
Sustained Peak Current	Icc-sp_6			3630.4	mA	
Supply Current	Icc-6			3508.8	mA	Steadystate
Case Temperature	TC	0	25	70	°C	

Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Note
Module Output (each lane, at TP4) [Note 1]					
Signaling Rate Per Lane(range)	-100ppm	26.5625	+ 100ppm	GBd	
AC Common-mode Output Voltage(RMS)			17.5	mV	
Differential Peak-to-peak Output Voltage			900	mV	
Near-end ESMW (Eye Symmetry Mask Width)	0.265			UI	
Near-end Eye Height,Differential	70			mV	
Far-end ESMW(Eye Symmetry Mask Width)	0.2			UI	
Far-end Eye Height,Differential	30			mV	
Far-end Pre-cursor ISI ratio	-4.5		2.5	%	
Differential Output Return Loss	Equation (83E-2)			dB	Note2
Common to Differential Mode Conversion Return Loss	Equation (83E-3)			dB	Note2
Differential Termination Mismatch			10	%	
Transition Time (20% to 80%)	9.5			ps	
DC Common Mode Voltage	-350		2850	mV	
Module Input (each lane)					
Signaling Rate Per Lane (range)	-100ppm	26.5625	+ 100ppm	GBd	
Differential Pk-pk Input Voltage Tolerance	900			mV	at TP1a
Differential Input Return Loss	Equation (83E-5)			dB	at TP1,Note2
Differential To Common Mode Input Returnloss	Equation (83E-6)			dB	at TP1,Note2
Differential Termination Mismatch			10	%	at TP1
ESMW (Eye Symmetry Mask Width)	0.22			UI	at TP1a
Eye Width	0.22			UI	at TP1a
Applied Pk-pk Sinusoidal Jitter	Table 120E–6			MHz,UI	at TP1a
Eye Height	32			mV	at TP1a
Single-ended Input Voltage Tolerance Range	-0.4		3.3	V	at TP1a
DC Common Mode Voltage	-350		2850	mV	at TP1

Notes:

[1] Electrical module output is squelched for loss of optical input signal.

[2] IEEE Std 802.3-2022 Section 6

Optical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Channel Data Rate	fDC		106.25		Gb/s	
Signaling Rate	fSG		53.125		GBd	PAM4
Signal Speed Variation From Nominal	ΔfSG	-100		+ 100	ppm	
Wavelength (Range)	λC	1304.5		1317.5	nm	
Side-mode Suppression Ratio	SMSR	30			dB	
Average Launch Power		-3.1		4.0	dBm	Note 1
Outer Optical Modulation Amplitude (OMAouter) [Figure 3]		-0.1 -1.5 +TDECQ	dBm	4.2	dBm	for TDECQ <1.4dB for 1.4 dB ≤TDECQ≤ 3.4dB
Transmitter And Dispersion Eye Closure For PAM4	TDECQ			3.4	dB	
Transmitter Eye Closure For PAM4	TECQ			3.4	dB	
|TDECQ– TECQ|				2.5	dB	
Over/Under-shoot				22	%	
Transmitter Power Excursion				2.0	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time				17	ps	
Average Optical Output Power Of Off Transmitter	Poff			-15	dBm	
RIN 15.6OMA				-136	dB/Hz	
Optical Return Loss Tolerance				17.1	dB	
Transmitter Reflectance				-26	dB	Note2
Average Receive Power		–7.1		4.0	dBm	Note3
Receive Power (OMAouter)				4.2	dBm	
Receiver Reflectance				-26	dB	for TECQ <1.4dB, Note 4
Receiver sensitivity (OMAouter) [Figure3]		Max -4.5 Max (-5.9 + TECQ)				
Stressed Receiver Sensitivity (OMAouter)				-2.5	dBm	Note 4,5
Conditions of stressed receiver sensitivity test (note 6)						
Stressed Eye Closure For PAM4 (SECQ)	SECQ			3.4	dB	

Note:

[1] Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

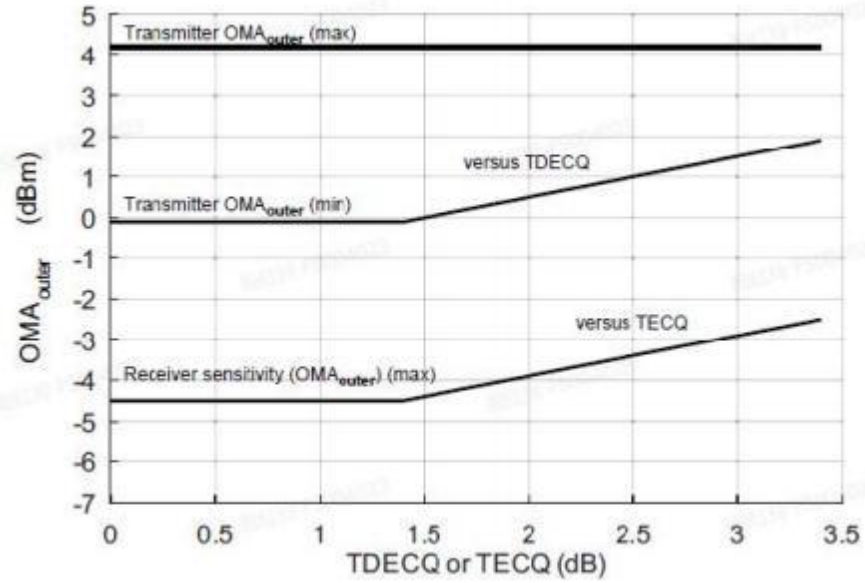
[2] Transmitter reflectance is defined looking into the transmitter.

[3] Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

[4] For when Pre-FEC BER is 2.4 x 10-4.

[5] Measured with conformance test signal at TP3 (see IEEE Std 802.3-2022 clause 140.7. 10) for the BER specified in IEEE Std 802.3c-2022 clause 140.1.1.

[6] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



QSFP-DD Edge Connector and Pinout Description

The electrical pinout of the QSFP-DD module is shown in Figure 2 below.

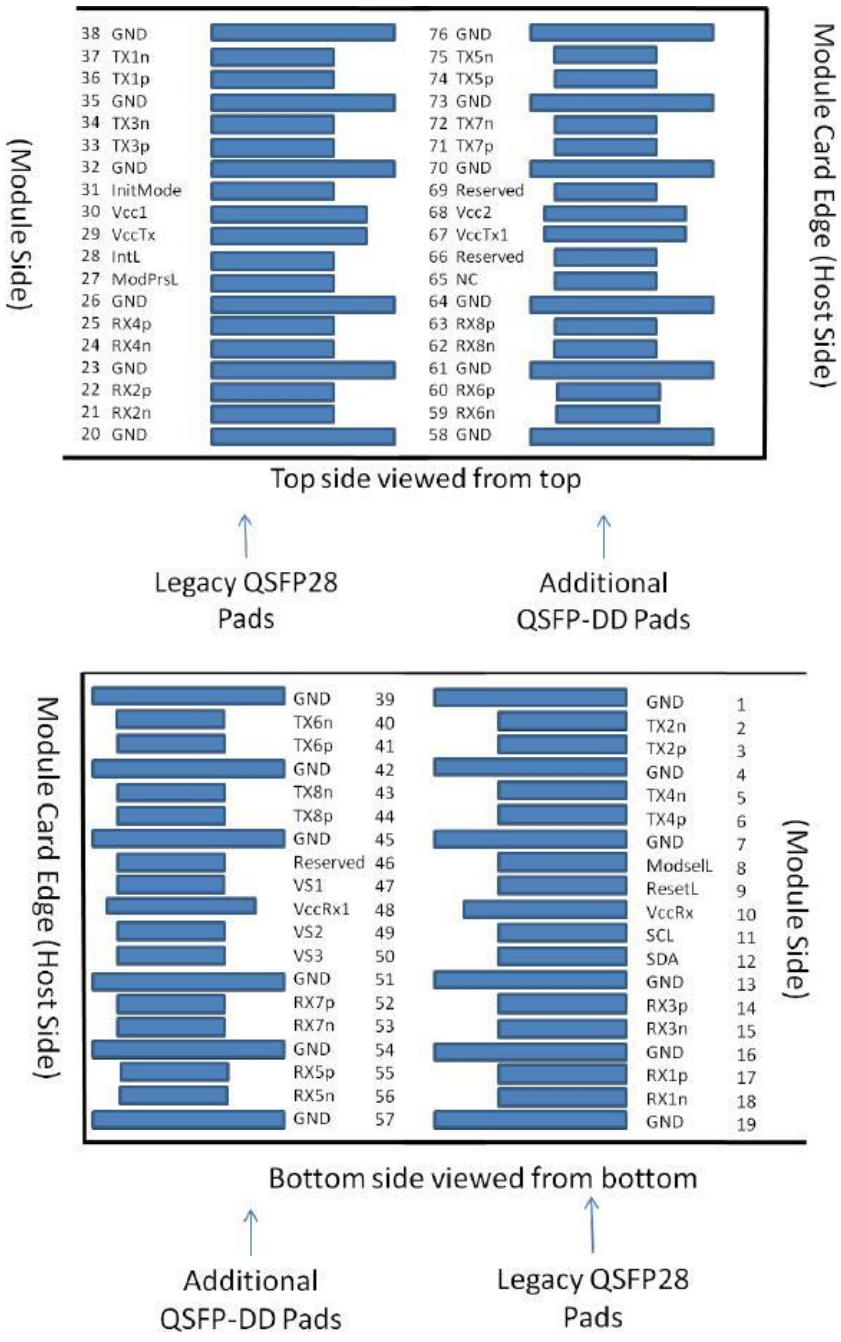


Figure 1. Host PCB QSFP-DD pad assignment top view

Pin No.	Symbol	Description	Note
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	Init Mode	Initialization mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Ground	1
39	GND	Ground	1

Pin No.	Symbol	Description	Note
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data output	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data output	
45	GND	Ground	1
46	Reserved	For Future Use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3V power supply	2
68	Vcc2	3.3V power supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Output	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Output	
76	GND	Ground	1

Note:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-

common ground plane;

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card

Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA;

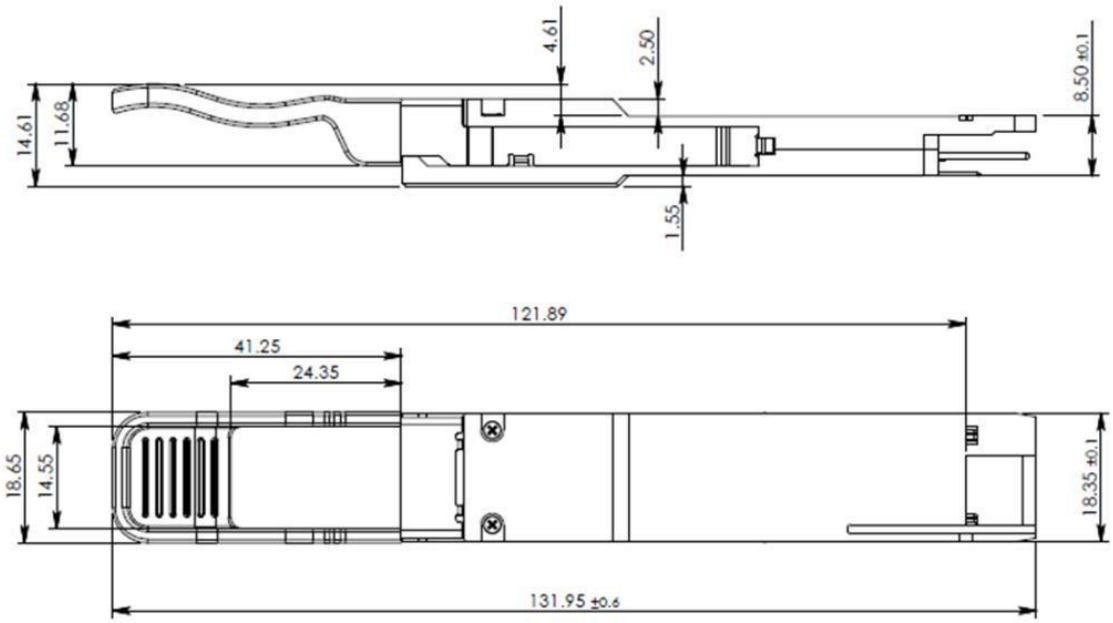
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10

kOhms and less than 100 pF;

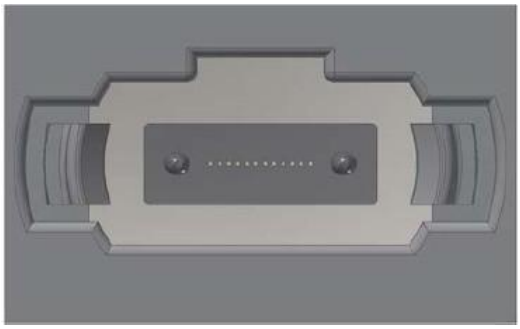
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur

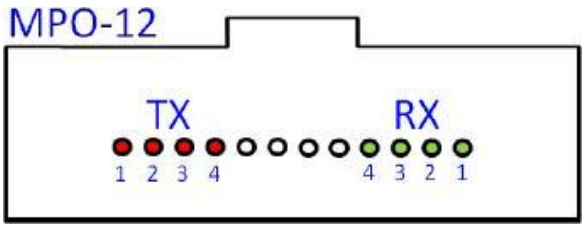
simultaneously, followed by 2A, 2B, followed by 3A,3B.

Mechanical Specifications



Optical Interface





Ordering information

Part Number	Product Description
LQD-M31400-FR1SC	400G, QSFP-DD, FR1, 2Km, 0~+70℃, MPO-12/APC, Silicon Photonics Transceiver