LQD-M31400-DR4SC

QSFP-DD400GBASE-DR4 1310nm 500m Silicon Photonics Transceiver

Product Features

- Compliant with QSFP-DD MSA
- Four Parallel 1310nm Optical Lanes
- IEEE 802.3bs 400GBASE-DR4 Specification Compliant
- Compliant with RoHS Requirement
- Up to 500m Transmission on Single Mode Fiber (SMF) with FEC
- 8x53.125Gb/s Electrical Interface (400GAUI-8)
- Data Rate 4* 106.25Gbps (PAM4) Optical Interface
- Case Temperature Range: 0 to 70°C
- Maximum Power Consumption 10W
- MPO-12/APC Connector
- Built-in Digital Diagnostic Functions
- Laser Safety Class 1

Applications

- 400G Ethernet
- InfiniBand Interconnects
- Data Center and Enterprise Networking

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Unit	Min	Typ	Max	Note
Storage Temperature	℃	-40		85	
Operating Relative Humidity	%	0		85	
Power Supply Voltage	V	-0.5		3.63	

Recommended Operating Conditions

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Unit	Min	Typ	Max	Note
Storage Temperature	℃	0		70	
Power Supply Voltage	V	3.135	3.3	3.465	
Power Consumption	W			10	
Pre-FEC Bit Error Ratio			2.4E-4		
Post-FEC Bit Error Ratio			1E-12		1
Link Distance	m	2		500	2

Note:

1. FEC is provided by host system;
2. FEC is required on host system to support maximum distance.

Electrical Characteristics

Parameter	Unit	Min	Typ	Max	Note
Transmitter					
Signaling Rate, each Lane	GBd	26.5625 ± 100 ppm			TP1
Data Input Swing Differential/TX	mV	85	-	1600	
Data Differential Impedance	Ω	90	100	110	
Receiver					
Signaling Rate, each Lane	GBd	26.5625 ± 100 ppm			TP4
Data Output Swing Differential/RX	mV		-	900	
Data Differential Impedance	Ω	90	100	110	

Optical Specifications

Parameter	Unit	Min	Typ	Max	Note
Transmitter					
Signaling rate, each lane	GBd	53.125 ± 100 ppm			PAM4
TX Central Wavelength	nm	1304.5	1310	1317.5	
Side-mode Suppression Ratio (SMSR)	dB	30			
Average Launch Power, each lane	dBm	-2.9		4	1
Outer Optical Modulation Amplitude (OMAouter), each lane	dBm	-0.8		4.2	2
Launch Power i n OMAouter minus TDECQ,each Lane(min)	dBm	-2.2			
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane (max)	dB			3.4	3
Average Launch Power of OFF Transmitter, each lane (max)	dBm			-15	
Extinction Ratio, each lane (min)	dB	3.5			
Optical Return Loss Tolerance (max)	dB			21.4	
RIN21.4OMA (max)	dB/Hz			-136	
Transmitter Reflectance (max)	dB			-26	
Receiver					
Signaling Rate, each Lane	GBd	26.5625 ± 100 ppm			TP4
RX Central Wavelength	nm	1304.5	1310	1317.5	
Damage Threshold (min)	dBm	5			4
Average Receive Power per Lane	dBm	-5.9		4.0	5
Receiving Power (OMAouter) per Lane	dBm			4.2	
Receiver Reflectance (max)	dB			-26	
Receiver Sensitivity (OMAouter), eachlane (max)	dBm	Equation (1)			6
Stressed Receiver Sensitivity (OMAouter)per Lane	dBm			-1.9	7
Conditions of Stressed Receiver Sensitivity Test					
Stressed Eye Closure for PAM4 (SECQ),lane under test	dB		3.4		8
OMAouter of each aggressor lane	dBm			4.2	
LOS Assert	dBm	-15			
LOS De-Assert	dBm			-8.9	
LOS Hysteresis	dB	0.5			

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance;

2. Even if the TDECQ < 1.4dB for an extinction ratio of ≥ 5dB or TDECQ < 1. 1dB for an extinction ratio of < 5dB, the OMAouter (min) must exceed the minimum value specified here;

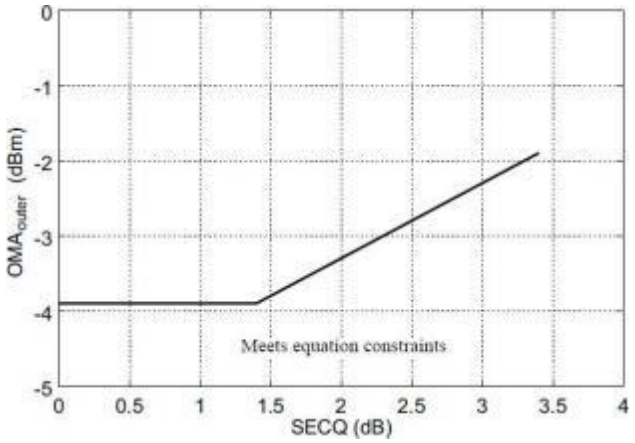
3. Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement;

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance;

5. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this

power level on one lane. The receiver does not have to operate correctly at this input power;

6. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation: RS=max (−3.9, SECQ−5.3), where RS is the receiver sensitivity, and SECQ is the SECQ of the transmitter used to measure the receiver sensitivity. which is illustrated in the Figure;

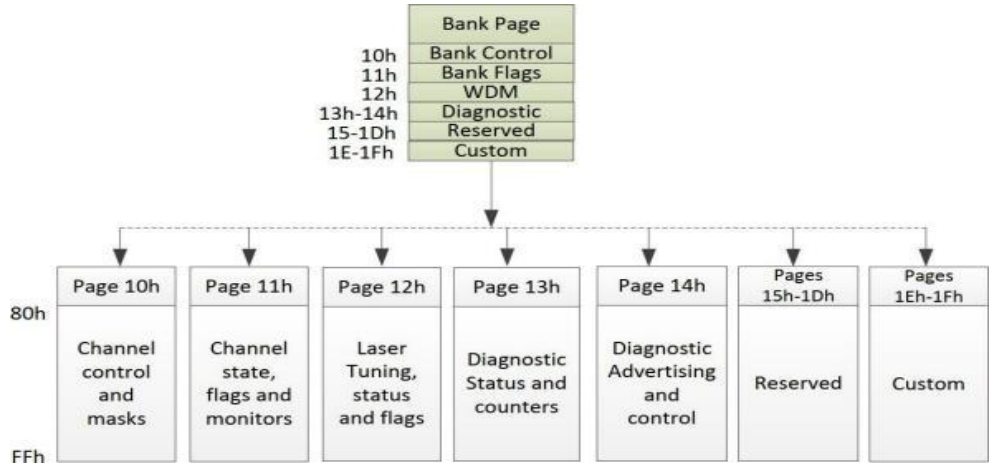


7. Measured with conformance test signal at TP3 for the BER equal to 2.4E-4;

8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Functions

Parameter	Unit	Error	Note
Temperature Monitor	℃	±3	1LSB= 1/256℃
Supply Voltage Monitor	V	±0.1	1LSB= 100uV
Bias Current Monitor	mA	± 10%	1LSB=2uA
TX Power Monitor	dBm	±3	1LSB=0.1uW
RX Power Monitor	dBm	±3	1LSB=0.1uW



QSFP-DD Edge Connector and Pinout Description

The electrical pinout of the QSFP-DD module is shown in Figure 2 below.

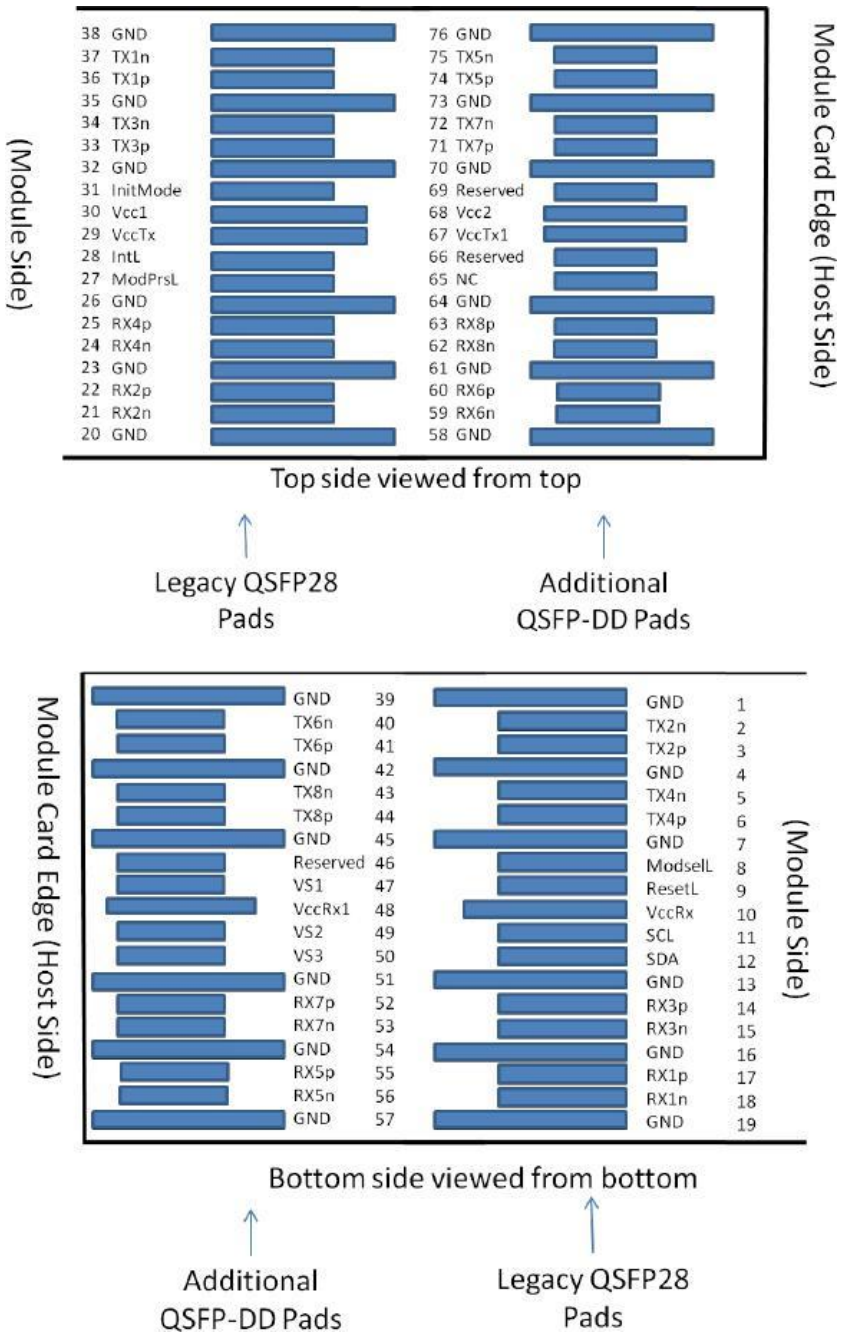


Figure 1. Host PCB QSFP-DD pad assignment top view

Pin No.	Symbol	Description	Note
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	Init Mode	Initialization mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Ground	1
39	GND	Ground	1

Pin No.	Symbol	Description	Note
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data output	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data output	
45	GND	Ground	1
46	Reserved	For Future Use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3V power supply	2
68	Vcc2	3.3V power supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Output	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Output	
76	GND	Ground	1

Note:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-

common ground plane;

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card

Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA;

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10

kOhms and less than 100 pF;

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur

simultaneously, followed by 2A, 2B, followed by 3A,3B.

Recommended Power Supply Filter

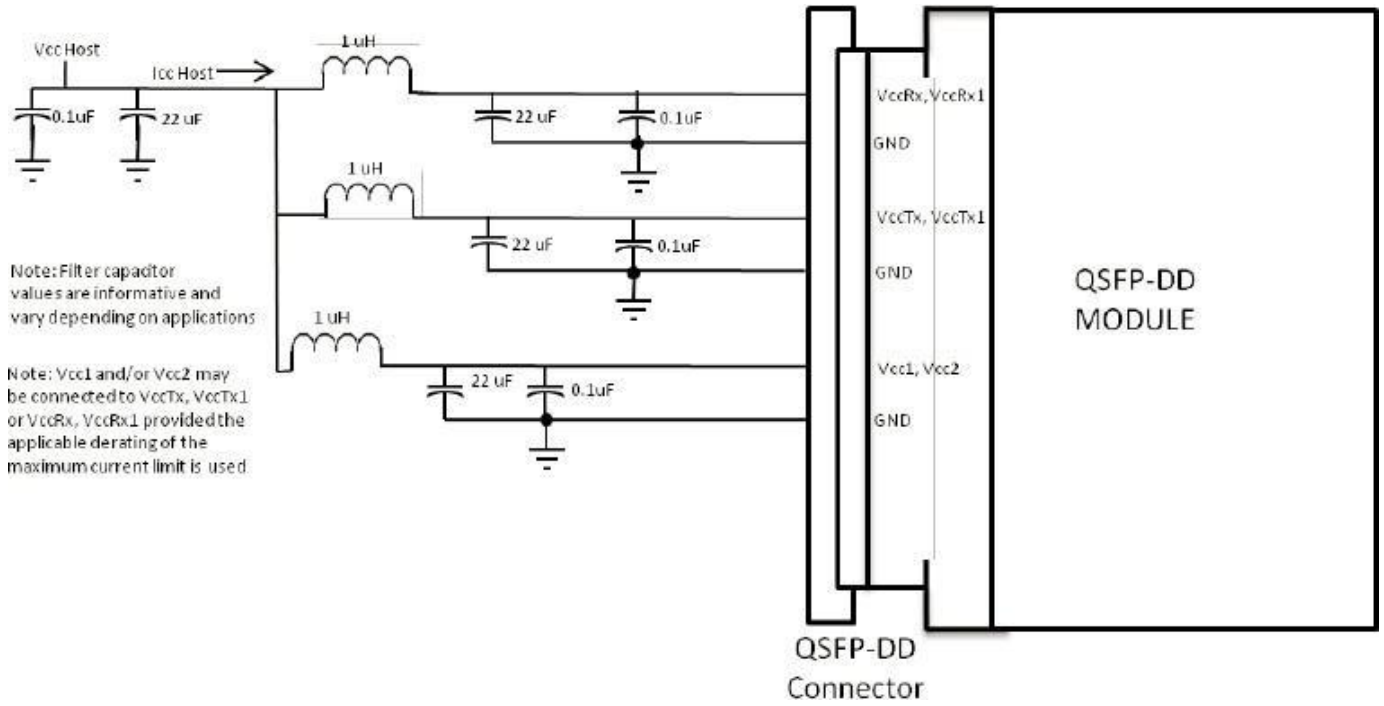
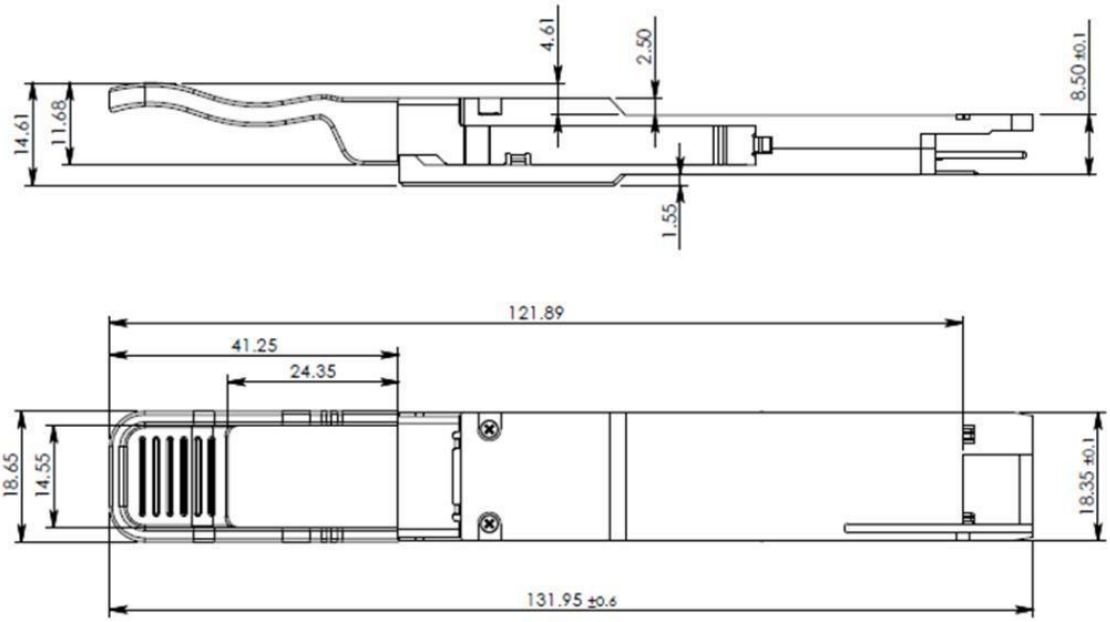
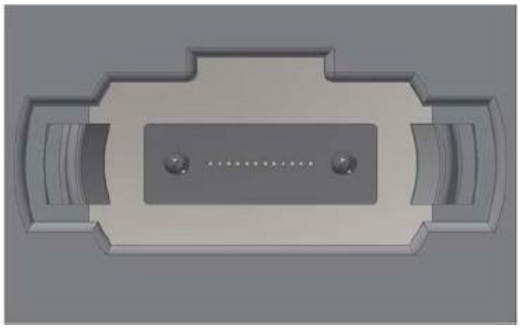


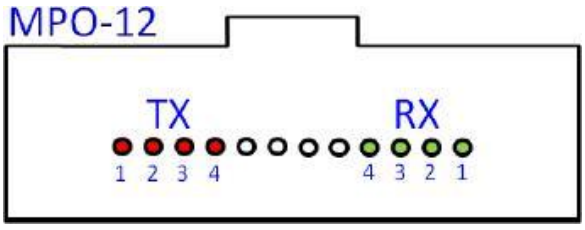
Figure 2. Recommended Power Supply Filter

Mechanical Specifications



Optical Interface





Ordering information

Part Number	Product Description
LQD-M31400-DR4SC	400G, QSFP-DD, DR4, 500m, 0~+70℃, MPO-12/APC, Silicon Photonics Transceiver