LQD-M31400-024C

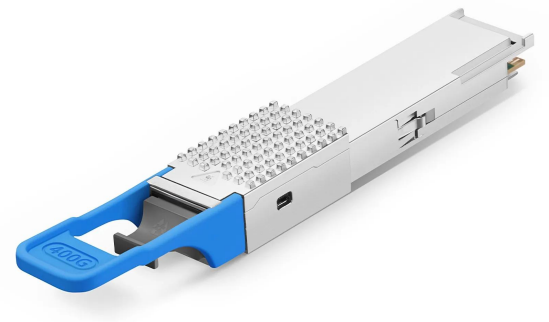
400GBASE-XDR4 QSFP-DD PAM4 1310nm MPO-12/APC 2km DOM Transceiver

Product Features

- Compliant with IEEE802.3bs Standard: -400GAUI-8 Electrical Interface
- Compliant with IEEE 802.3cu Standards: -4x 100GBASE-FR1 Optical Interface
- Compliant with QSFP-DD MSA HW Rev 5.1 Type 2 Housing with MPO-12 Connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

Applications

- 400GBASE-DR4+



Descriptions

The 400GBASE-XDR4 Module supports link lengths of up to 2km parallel SMF with MTP/MPO-12 connector. It is compliant to IEEE
802.3bs protocol and 400GAUI-8 standards. The 400 Gigabit Ethernet signal is carried over four parallel lanes by one wavelength per lane. It can be used as 4x100G breakout to QSFP28-FR-100G.

Recommended Operating Conditions

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	TOP	0	-	70	ºC
Storage Temperature	TS	-40	-		ºC
Supply Current	Ts	-	-	3827.8	mA
Power Supply Voltage	VCC	3.13	3.3	3.46	V
Instantaneous Peak Current at Hot Plug	ICC_IP	-	-	4000	mA
Sustained peak Current at Hot Plug	ICC_SP	-	-	3300	mA
Maximum Power Dissipation	PD	-	-	10	W
Aggregate Bit Rate	ABR	-	425	-	Gb/s
Channel Data Rate	fDC	-	106.25	-	Gb/s
Signalling Rate Per Lane	SRL	-	53.125	-	GBd
Operating Distance	-	2	-	2000	m

Optical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Center Wavelength, Per Lane	λC	1304.5	1311	1317.5	nm
Side-mode Suppression Ratio	SMSR	30	-	-	dB
Average Launch Power, Each Lane	POUTL	-3.1	-	4	dBm
Optical Modulation Amplitude, Each Lane*1	OMA	-	-	4.2	dBm
Average Launch Power Tx_Off, Each Lane	POUT_OFF	-	-	-40	dBm
Launch power in OMAouter Minus TDECQ	-				dBm
Transmitter and Dispersion Eyeclosure for PAM4	TDECQ	-		3.4	dB
RIN17.1OMA	RIN	-	-	-136	dB/Hz
Optical Return Loss Tolerance	ORL	-	-	17.1	dB
Extinction Ratio	ER	3.5	-	-	dB
Optical Return Loss Tolerance	-	-	-	17.1	dB
Transmitter Reflectance	-	-	-	-26	dB
Receiver					
Center Wavelength, Per Lane	λC	1304.5	1311	1317.5	nm
Damage Threshold, Each Lane	PMAX	5.0	-	-	dBm
Receiver Sensitivity (OMA)* 1	BOL	-	-	-4.2	dBm
Stressed Receiver Sensitivity in OMA* 1	SRS	-	-	-2.5	dBm
Stressed Eye Closure for PAM4(SECQ), Lane Under Test	SECQ	-	3.4	-	dB
OMAouter of Each Aggressor Lane	-	-		-	dBm
Receiver Loss of Signal Indicator Assert	RX_LOSA	-	-		dBm

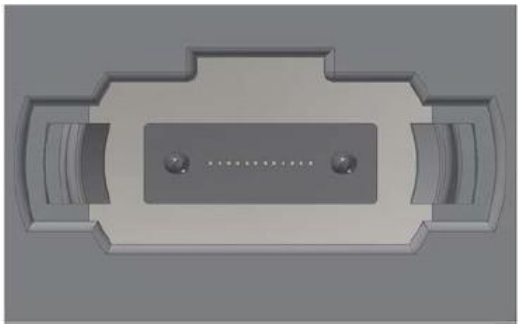
Parameter	Symbol	Min	Typical	Max	Unit
Level					
Receiver Loss of Signal Indicator Deassert Level	RX_LOSD	-	-		dBm
Hysteresis	-	0.5	-	4	dB

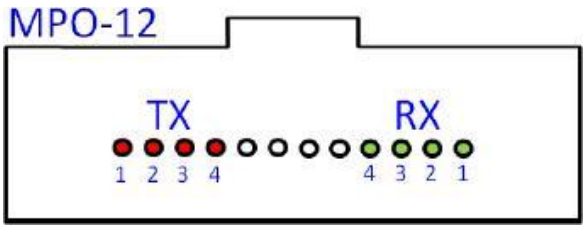
Notes:
1. Measured with conformance test signal at TP3 for the BER = 2.4x10-4.

Digital Diagnostic Monitoring Specifications

Parameter	Symbol	Min.	Typ.
Temperature	0 to 70	3	ºC
Voltage	3.13 to 3.46	±3%	V
Tx Bias Current	2 to 100	± 10%	mA
Tx Output Power	-3.1 to 4	±2	dB
Rx Power	-7.1 to 4	±2	dB

Optical Interface





QSFP-DD Edge Connector and Pinout Description

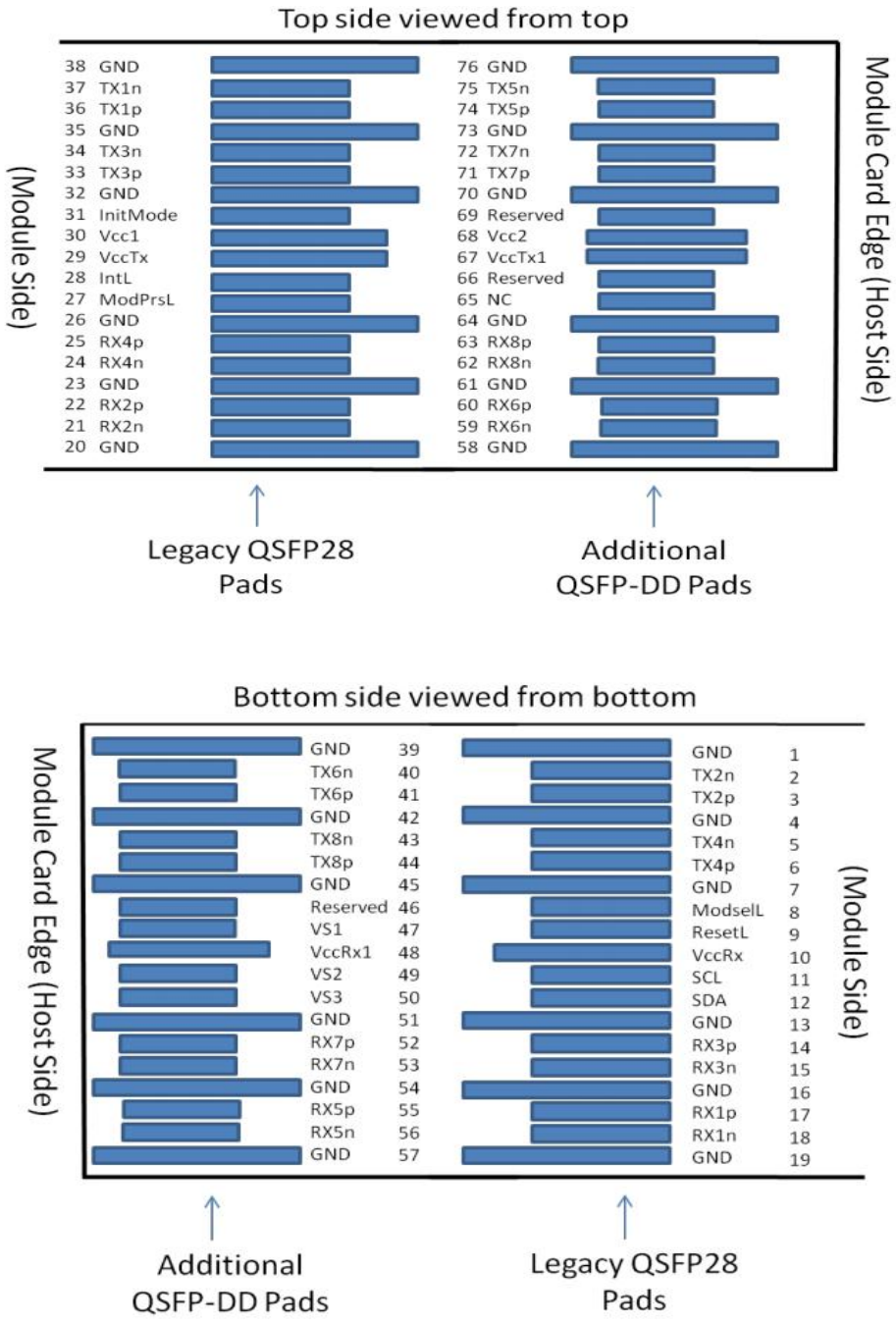


Figure 1. Host PCB QSFP-DD pad assignment top view

Pin No.	Symbol	Description	Note
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	Init Mode	Initialization mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Ground	1
39	GND	Ground	1

Pin No.	Symbol	Description	Note
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data output	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data output	
45	GND	Ground	1
46	Reserved	For Future Use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3V power supply	2
68	Vcc2	3.3V power supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Output	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Output	
76	GND	Ground	1

Note:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-

common ground plane;

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card

Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA;

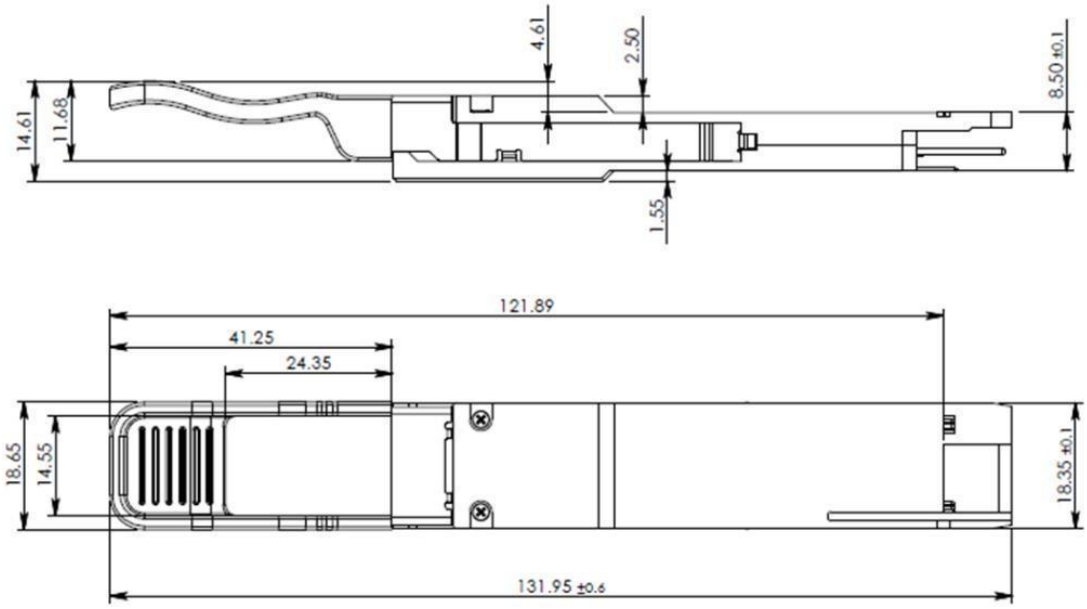
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10

kOhms and less than 100 pF;

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur

simultaneously, followed by 2A, 2B, followed by 3A,3B.

Mechanical Specifications



Ordering information

Part Number	Product Description
LQD-M31400-024C	400Gbps, QSFP-DD DR4+, 2Km, 0~+70° C, MPO-12/APC, with DDM