LQD-LW400-ER8C

400G QSFP-DD PAM4 LWDM ER8 40km LC SMF Transceiver

Product Features

- Compliant with IEEE std 802.3cnTM-2019:
  - 400GBASE-ER8 optical interface
  - 400GAUI-8 electrical interface
- Compliant with QSFP-DD MSA HW Rev 5.1 with duplex LC connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Case operating temperature 0° C to 70° C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1/1M Laser

Applications

- 400G Ethernet
- Data Center Interconnect
- Infiniband Interconnect
- Enterprise Networking

Standards

- IEEE 802.3cd
- QSFP-DD MSA
- CMIS4.0

Descriptions

LQD-LW400-ER8C is a transceiver module designed for 40km optical communication applications, and it is compliant to 50G Lambda MSA standard. This module can convert 8-channel 53.125Gb/s electrical data to 8-channel optical signals, and multiplex them into a single channel for 425Gb/s optical transmission. Similarly, it optically de-multiplexes a 425Gb/s input into 8-channel signals, and converts them to 8-channel output electrical data on the receiver side. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	T_{STG}	-40	+85	°C
Supply Voltage	V_{CC}	0	4	V
Relative Humidity	RH	10% to 90% non-condensing		

Operating Conditions

Parameter	Symbol	Min	Max	Units
Case Temperature- Operating	TCASE	0	70	°C
Supply Voltage	Vcc	3.14	3.46	V
Power Consumption	PDISS		14	W
Pre-FEC Bit Error Ratio			2.4x10^-4	
Link Distance	2		40000	M

Optical Characteristics

Transmitter Parameter	Symbol	Min	Typical	Max	Units	Notes
Lane Wavelength Range	λ_{C0}	1272.55	1273.55	1274.54	nm	
	λ_{C1}	1276.89	1277.89	1278.89	nm	
	λ_{C2}	1281.25	1282.26	1283.27	nm	
	λ_{C3}	1285.65	1286.67	1287.68	nm	
	λ_{C4}	1294.53	1295.56	1296.59	nm	
	λ_{C5}	1299.02	1300.06	1301.09	nm	
	λ_{C6}	1303.54	1304.59	1305.63	nm	
	λ_{C7}	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Signal rate per lane	DRL	-	26.5625	-	GBd	
Average launch Power per lane	AOPL	-0.6	-	5.6	dBm	1
Total Average launch power	AOPT	-	-	14.6	dBm	
Outer Optical Modulation Amplitude (OMAouter) each lane	TOMA	2.4	-	6.4	dBm	
Difference in launch power between any two lanes (OMAouter)	D_{T_OMA}	-	-	4	dB	
Launch Power in OMAouter minus TDECQ, each lane	TOMA-TDECQ	1	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
TTDECQ – 10log10(Ceq)	-	-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-30	dBm	
Extinction Ratio	-	6	-		dB	
Relative Intensity Noise (OMA)	-		-	-136	dB/Hz	
Side-Mode Suppression Ration (SMSR)	-	30	-	-	dB	
Optical Return Loss Tolerance	-	-	-	15.6	dB	
Transmitter Reflectance	-	-	-	-26	dB	2
Transmitter over/under-shoot	-	-	-	25	%	
Transmitter peak-to-peak power	-	-	-	5.2	dBm	
Transmitter transition time	-	-	-	17	ps	

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength
Note 2: Transmitter reflectance is defined looking into the transmitter

Receiver Optical Specifications

Receiver Parameter	Lane	Min	Typical	Max	Units	Notes
Lane Wavelength Range	λ_{C0}	1272.55	1273.55	1274.54	nm	
	λ_{C1}	1276.89	1277.89	1278.89	nm	
	λ_{C2}	1281.25	1282.26	1283.27	nm	
	λ_{C3}	1285.65	1286.67	1287.68	nm	
	λ_{C4}	1294.53	1295.56	1296.59	nm	
	λ_{C5}	1299.02	1300.06	1301.09	nm	
	λ_{C6}	1303.54	1304.59	1305.63	nm	
	λ_{C7}	1308.09	1309.14	1310.19	nm	
Damage Threshold, each Lane	AOPD	-3.4	-	-	dBm	
Average Receive Power, each Lane	AOPR	-18.6	-	-4.4	dBm	
Receive Power (OMAouter), each Lane	OMAR	-	-	-3.6	dBm	
Difference in Receive Power between any two Lanes (OMAouter)	DR_OMA	-	-	5.8	dB	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMAouter), each Lane	SOMA	-	-	Max(－16.1, SECQ – 17.5)	dBm	1
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-14.1	dBm	2
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under test	-	-	3.4	-	dB	
SECQ － 10log10(Ceq), lane under test	-	-	-	3.4	dB	
OMAouter of each aggressor lane	-	-	-8.3		dBm	

Note 1: Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 1.4 dB.
Note 2: Measured with conformance test signal at TP3 for the BER = 2.4x10-4

Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Notes
Receiver electrical output characteristics at TP4					
Signaling rate per lane		26.5625		GBd	
AC common-mode output voltage(RMS)		-	17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265		UI	
Near-end Eye height, differential	70			mV	
Near-end vertical eye closure			7.5	dB	
Far-end ESMW (Eye symmetry mask width)		0.20		UI	

Far-end Eye height, differential	30			mV	
Far-end vertical eye closure			7.5	dB	
Far-end pre-cursor ISI ratio	-4.5		2.5	%	
Common mode to differential conversion return loss	802.3 Equation(83E-3)			dB	
Differential output return loss	802.3 Equation(83E-2)			dB	
Differential termination mismatch			10	%	
Transition time (min, 20% to 80%)		9.5		ps	
DC common mode voltage	-350		2850	mV	
Transmitter electrical input characteristics at TP1					
Signaling rate, per lane		26.5625		GBd	
Differential peak-to-peak input voltage tolerance	900			mV	
Differential input return loss	802.3 Equation(83E-5)				
Differential to common mode input return loss	802.3 Equation(83E-6)			mV	
AC common-mode output voltage(RMS)			17.5	mV	
Single-ended voltage tolerance range	-0.4		3.3	V	
Module stressed input	802.3 120E.3.4.1			UI	
Differential termination mismatch			10	%	
DC common mode voltage	- 350			mV	

Digital Diagnostic Monitoring Specifications

Parameters	Unit	Specification
Temperature Monitor absolute error	°C	±3
Supply Voltage Monitor absolute error	%	±5
I_bias Monitor absolute error	%	±10
Received Power (Rx) Monitor absolute error	dB	±3.0
Transmit Power (Tx) Monitor absolute error	dB	±3.0

QSFP-DD Edge Connector and Pinout Description

The electrical pinout of the QSFP-DD module is shown in Figure 1 below.

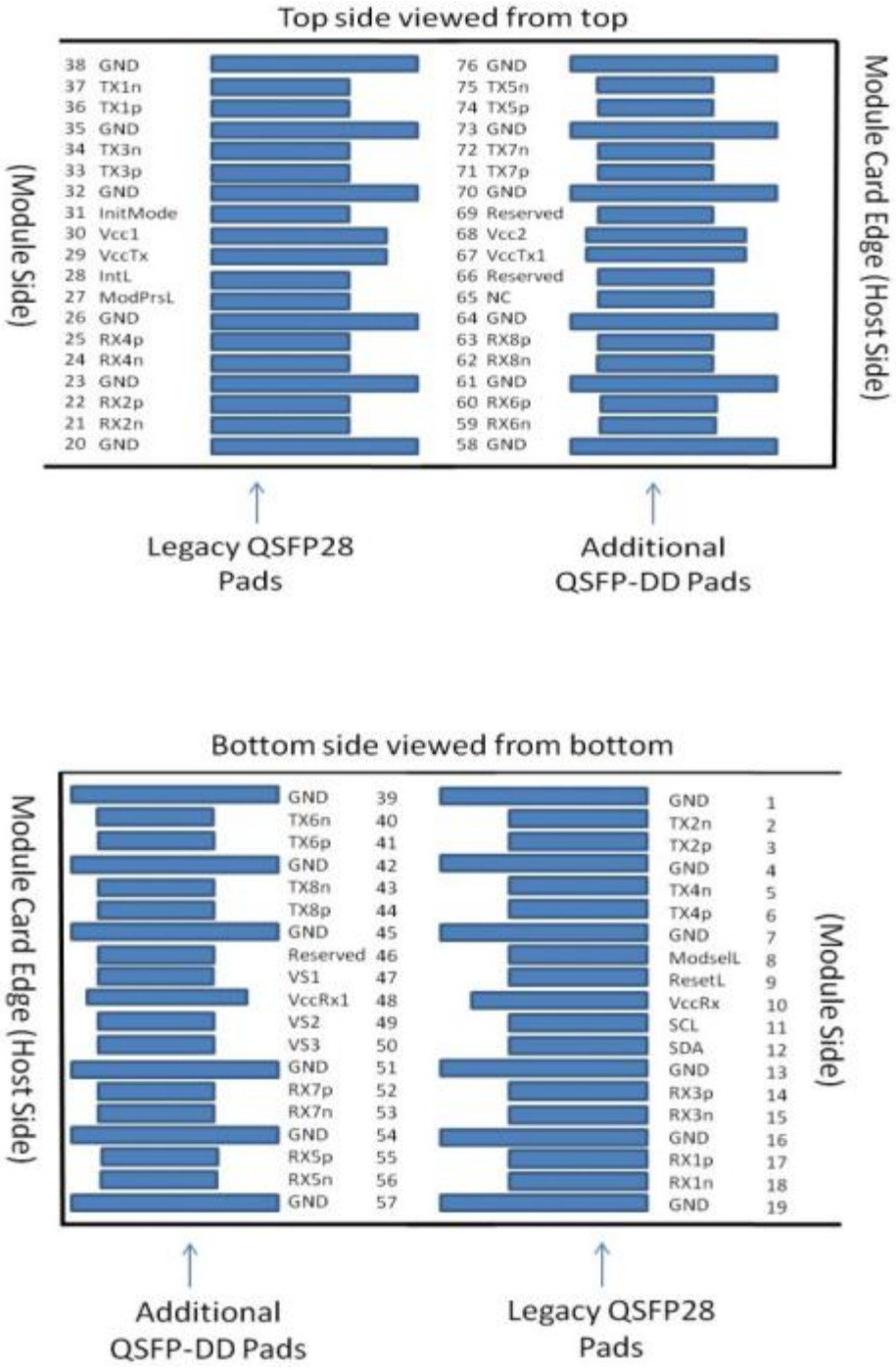


Figure 1. Host PCB QSFP-DD pad assignment top view

Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	TWI serial interface clock	3B	
12	LVCMOS-I/O	SDA	TWI serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
46	LVCMOS /CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500 mA.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500 mA.

Note 3: Reserved and no Connect pads recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note 5: Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10 kΩ.

Note 6: ePPS/Clock if not used recommended to be terminated with 50 Ω to ground on the host.

Module Block Diagram

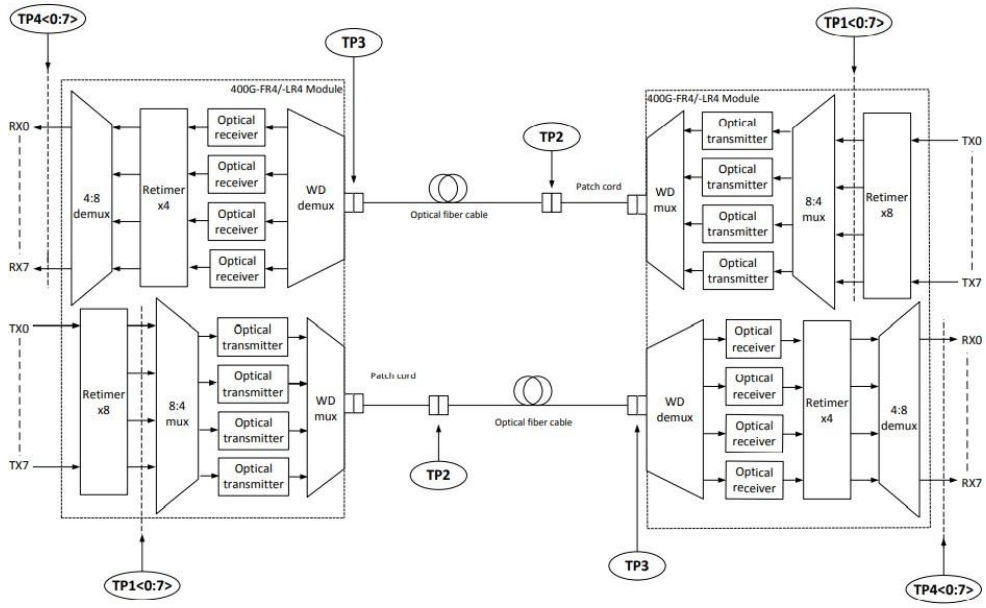
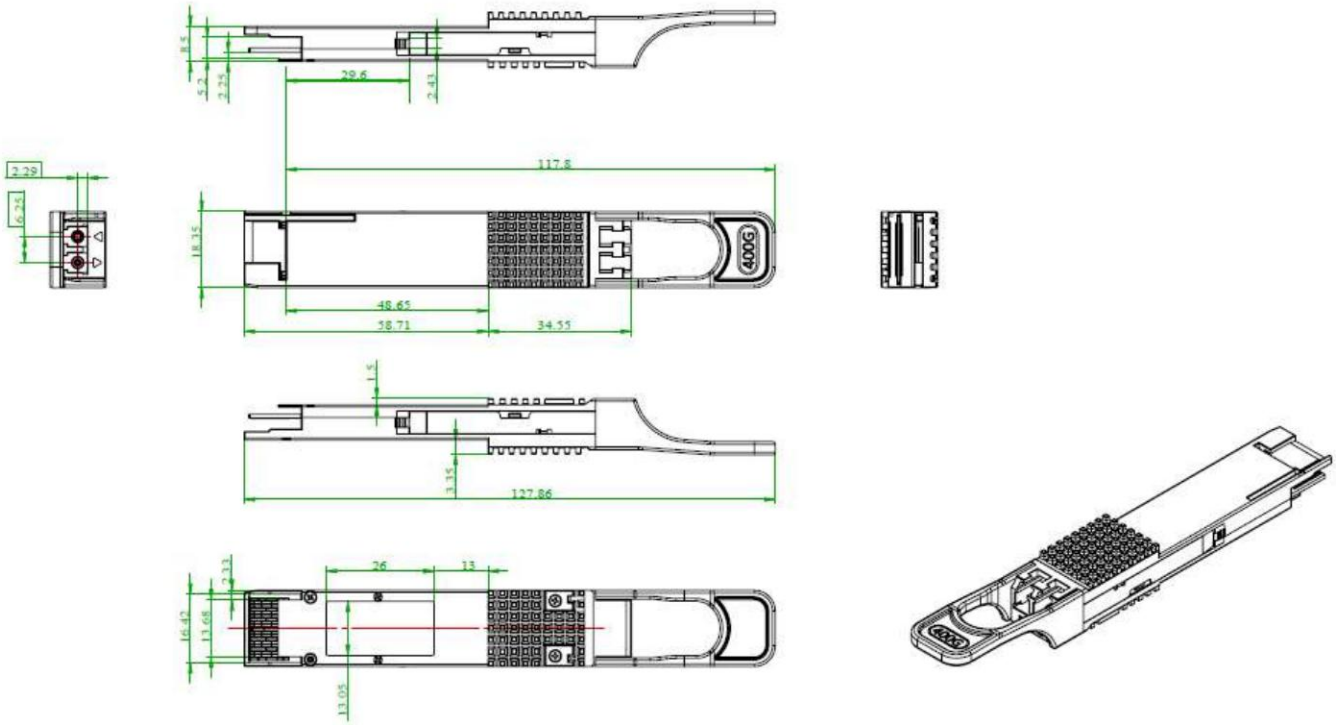


Figure 2. Module Block Diagram

Memory map

Compatible with CMIS 5.1

Mechanical Specifications



Ordering information

Part Number	Product Description
LQD-LW400-ER8C	400Gbps, LWDM, QSFP-DD, ER8, 40km, 0° C~+70° C, LC, with DDM