LQD-DM85800-SR8C

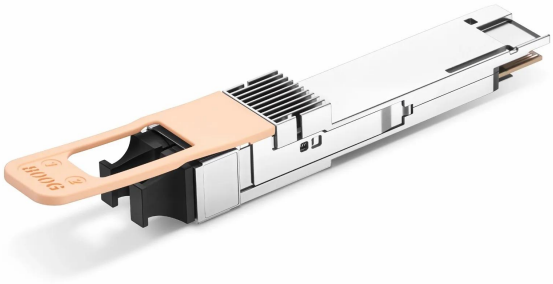
800GBASE-SR8 QSFP-DD 850nm 50m Dual MPO-12/APC
DOM Optical Transceiver

Product Features

- Up to 106.25 Gbps Data Rate Per Channel by PAM4 Modulation on Media Side
- Up to 106.25 Gbps Data Rate Per Channel by PAM4 Modulation on Host Side
- Dual MPO-12/APC Optical Interface
- Single +3.3V Power Supply
- DDM Function Implemented
- Hot-pluggable QSFP-DD Form Factor
- Maximum Link Length of 50M on OM4 MMF
- Power Consumption: <16W
- International Class 1 Laser Safety Certified
- Operating Temperature Range: 0℃ ~ +70℃
- Compliant with ROHS2.0

Applications

- 800GBASE Ethernet
- Switch & Router Connections
- Data Centers
- Other 800G Interconnect Requirements



Standards

- IEEE 802.3df
- IEEE P802.3ck™/D3.0
- QSFP-DD HW Rev 6.2
- CMIS Rev 4.0 or Later Version

Description

The 800G QDD-SR8-800G dual MPO-12/APC transceiver is designed to transmit and receive serial optical data links up to 106.25 Gbps data rate (per channel) by PAM4 modulation format over multi-mode fiber. It is a small-form-factor hot pluggable transceiver module integrated with the high performance VCSEL laser and high sensitivity PIN receiver. It is compliant with 800G Ethernet specs and QSFP-DD MSA.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	TS	-40	85	℃
Supply Voltage	VCC	-0.5	3.6	V
Relative Humidity (Non-condensing)	RH	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Note
Operating Case Temperature	TOPR	25		70	℃	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Media Side Bit Rate (Per channel)	BR		106.25		Gbps	
Host Side Bit Rate (Per channel)	BR		106.25		Gbps	

Optical Characteristics

The following table list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter(Per Lane)						
Signaling Rate, Each Lane (Range)		53.125 ± 100 ppm			GBd	
Modulation Format	PAM4					
Wavelength	λC	840		870	nm	
RMS Spectral Width	RMS			0.65	dB	
Average Launch Power, Each Lane	AOPL	-4.6		4	dBm	

Outer Optical Modulation Amplitude (OMAouter), Each Lane for Max (TECQ, TDECQ) <= 1.8 dB for 1.8 < Max (TECQ, TDECQ) <= 4.4 dB	OMAouter	-2.6		3.5	dBm	
Outer Optical Modulation Amplitude (OMAouter), EachLane (min) for 1.8<Max (TECQ,TDECQ)≤4.4 dB	OMAouter	-4.4+max (TECQ, TDECQ)		3.5	dBm	
Transmitter Excursion, Each Lane	DPx			2.3	dB	
Optical Extinction Ratio	ER	2.5			dB	
Transmitter and Dispersion Penalty Eye Closure for PAM4, Each Lane	TDECQ			4.4	dB	
Transmitter Transition Time	Tr 、 Tf			17	ps	
RIN14OMA				-132	dB/HZ	
Encircled Flux	FLX	>=86% at 19μm <=30% at 4.5μm			dBm	
Optical Return Loss Tolerance	ORL			14	dB	
Average Launch Power of OFF Transmitter, Each Lane				-30	dBm	
Receiver(Per Lane)						
Signaling Rate, Each Lane (Range)		53.125 ± 100 ppm			GBd	
Modulation Format	PAM4					
Wavelength	λC0	840		870	nm	
Damage Threshold, Each Lane	AOPD	5			dBm	
Average Receive Power, Each Lane	AOPR	-6.3		4	dBm	
Receive Power (OMAouter), Each Lane	OMAR			3.5	dBm	
Receiver Reflectance	RR			-15	dB	
Receiver Sensitivity (OMAouter) for TECQ ≤ 1.8 dB for 1.8 < TECQ ≤ 4.4 dB				-4.4 -6.2+TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), Each Lane	SRS			-1.8	dBm	1
Los Assert	LOS_A		-11		dBm	
Los De-assert	LOS_D		-10		dBm	

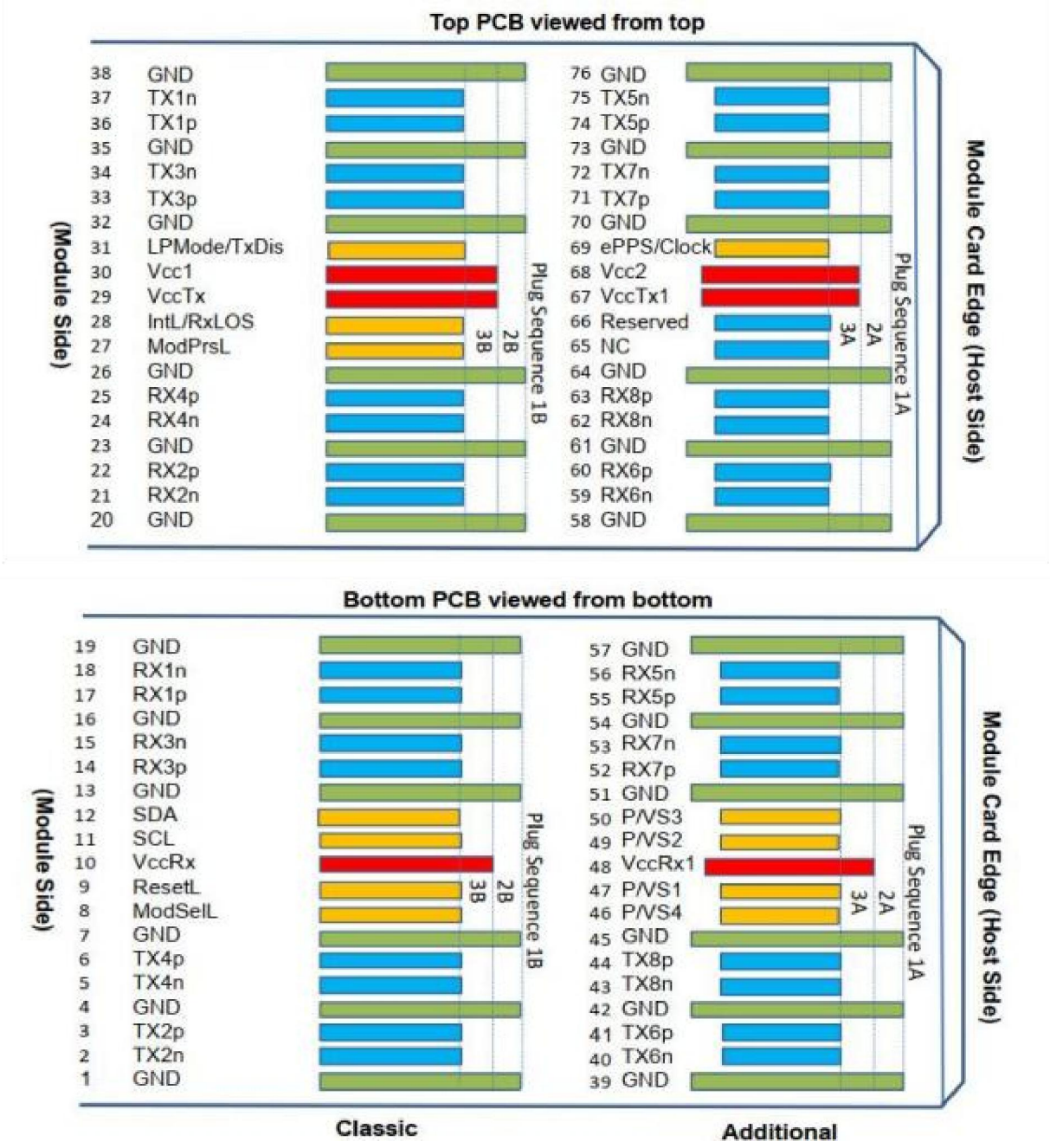
Notes:

1. BER = 2.4E-4

Electric Ports Definition

Parameter	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	3.135		3.465	V	
Signaling Rate, Each Lane	53.125 -50 ppm	53.125	53.125 +50 ppm	GBd	
Module Input Characteristics					
Differential Peak-to-peak Input Voltage Tolerance	750			mV	TP1a
Peak-to-peak AC Common-mode Voltage Tolerance Low-frequency, VCMLF	32			mV	TP1a
Full-band, VCMFB	80			mV	TP1a
Differential-mode to Common-mode Return Loss, RLcd	See IEEE Std 802.3ck™-2022 Equation (120G-2)			dB	TP1
Effective Return Loss, ERL	8.5			dB	TP1
Differential Termination Mismatch			10	%	TP1
Module Stressed Input Tolerance	See IEEE Std 802.3ck™-2022 120G.3.4.3				TP1a
Single-ended Voltage Tolerance	-0.4		3.3	V	TP1a
DC Common-mode Voltage Tolerance	-0.35		2.85	V	TP1
Module Output Characteristics					
Peak-to-peak AC Common-mode Voltage Low-frequency, VCMLF			32	mV	TP4
Full-band, VCMFB			80	mV	TP4
Differential Peak-to-peak Output Voltage Short Mode			600	mV	TP4
Long Mode			845	mV	TP4
Eye Height	15			mV	TP4
Vertical Eye Closure, VEC			12	dB	TP4
Common-mode to Differential- Mode Return Loss, RLdc	See IEEE Std 802.3ck™-2022 Equation(120G-1)			dB	TP4
Effective Return Loss, ERL	8.5			dB	TP4
Differential Termination Mismatch				%	TP4
Transition Time	8.5			ps	TP4
DC Common-mode Voltage Tolerance	-0.35		2.85	V	TP4
IIC Communication					
IIC Clock Frequency	100		1000	kHZ	
Clock Stretching			500	μs	
Data In Hold Time	0			μs	
Data In Setup Time	0.1			μs	

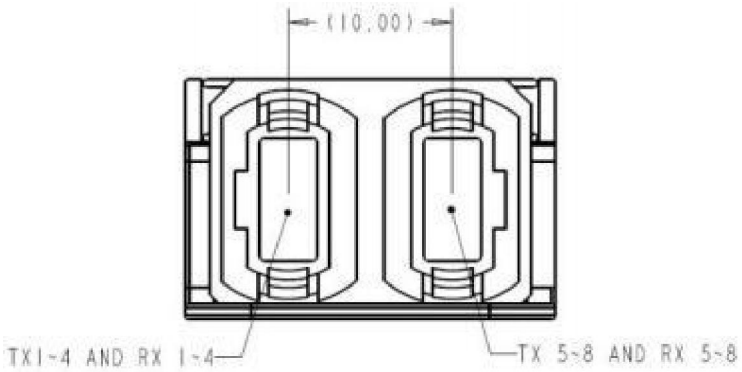
Pin Description



Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	TX2n	Transmitted Inverted Data Input
3	CML-I	TX2p	Transmitted Non-Inverted Data Input
4		GND	Ground
5	CML-I	TX4n	Transmitted Inverted Data Input
6	CML-I	TX4p	Transmitted Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VCC RX	+3.3 VDC Power Supply Receiver
11	LVCMOS-I/O	SCL	TWI Serial Interface Clock
12	LVCMOS-I/O	SDA	TWI Serial Interface Data
13		GND	Ground
14	CML-O	RX3p	Receiver Non-Inverted Data Output
15	CML-O	RX3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	RX 1p	Receiver Non-Inverted Data Output
18	CML-O	RX 1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	RX2n	Receiver Inverted Data Output
22	CML-O	RX2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	RX4n	Receiver Inverted Data Output
25	CML-O	RX4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/RXLOS	Interrupt/Optional RxLOS
29		VCC TX	+3.3 V Power Supply Transmitter
30		VCC1	+3.3 V Power Supply
31	LVTTL-I	LPMode/TXDis	Low Power Mode/Optioanl TX Disable
32		GND	Ground
33	CML-I	TX3p	Transmitted Non-Inverted Data Input
34	CML-I	TX3n	Transmitted Inverted Data Input
35		GND	Ground
36	CML-I	TX 1p	Transmitted Non-Inverted Data Input
37	CML-I	TX 1n	Transmitted Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	TX 6n	Transmitter Inverted Data Input
41	CML-I	TX 6p	Transmitter Non-inverted Data Input
42		GND	Ground
43	CML-I	TX 8n	Transmitter Inverted Data Input

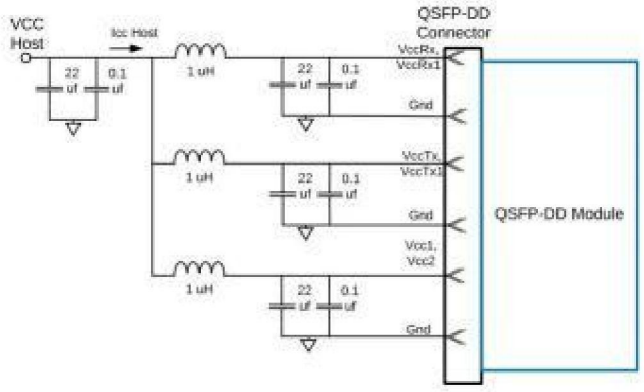
44	CML-I	TX 8p	Transmitter Non-inverted Data Input
45		GND	Ground
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1
48		VCC RX 1	3.3V Power Supply
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3
51		GND	Ground
52	CML-O	RX 7p	Receiver Non-inverted Data Output
53	CML-O	RX 7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	RX 5p	Receiver Non-inverted Data Output
56	CML-O	RX 5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	RX 6n	Receiver Inverted Data Output
60	CML-O	RX 6p	Receiver Non-inverted Data Output
61		GND	Ground
62	CML-O	RX 8n	Receiver Inverted DataOutput
63	CML-O	RX 8p	Receiver Non-inverted Data Output
64		GND	Ground
65		NC	Not Connected
66		Reserved	
67		VCCTX 1	3.3V Power Supply
68		VCC2	3.3V Power Supply
69	LVCMOS-I	ePPS/Clock	1PPS PTP Clock or Reference Clock Input
70		GND	Ground
71	CML-I	TX7p	Transmitter Non-inverted Data Input
72	CML-I	TX7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	TX5p	Transmitter Non-inverted Data Input
75	CML-I	TX5n	Transmitter Inverted Data Input
76		GND	Ground

Optical Interface

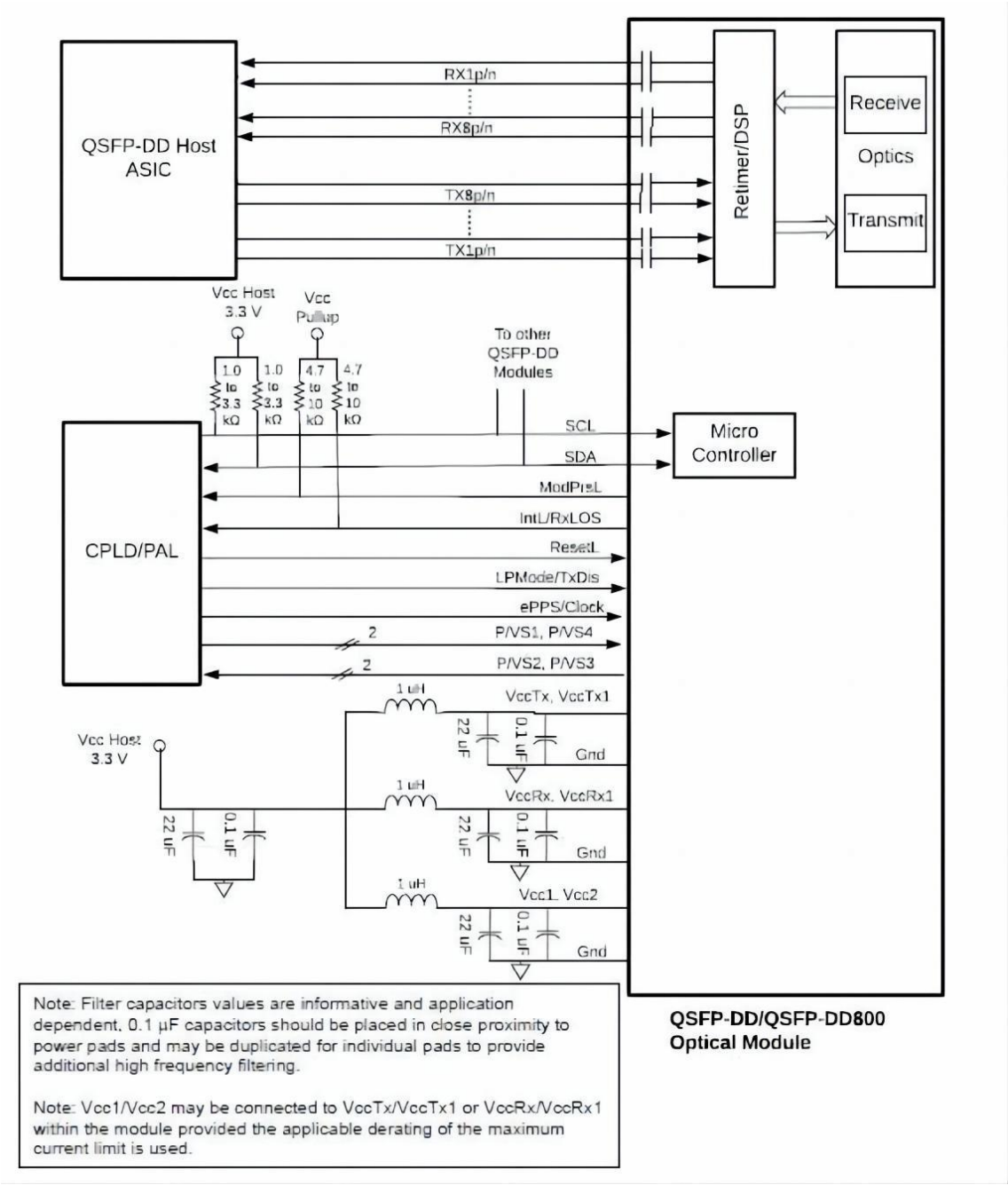


Host Board Power Supply Filtering

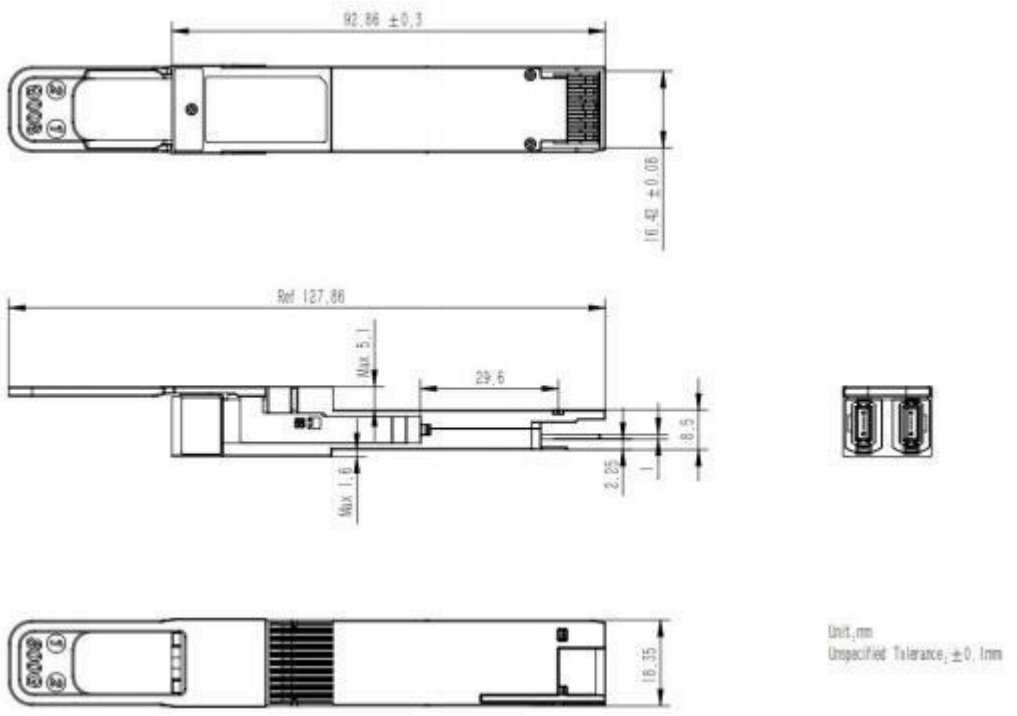
Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. System designers should choose components with appropriate DCR and ESR, to minimize the voltage drop and the amount of noise coupled to the module. Hosts supporting higher power classes modules may require additional design considerations, in order to minimize the voltage drop and the amount of noise coupled to the module.



Principle Diagram



Package Outline



Ordering information

Part Number	Product Description
LQD-DM85800-SR8C	800G, Dual MPO-12/APC, 850nm, QSFP-DD, 2xSR4/SR8, 50m, 0° C~+70°C, with DDM
LQD-M85800-SR8C	800G, MPO-16/APC, 850nm, QSFP-DD, SR8, 50m, 0° C~+70°C, with DDM