LQD-DM31800-DR8C

800G QSFP-DD DR8 Dual MPO-12/APC Transceiver

Product Features

- Compliant with IEEE 802.3cu-2021: 8x100GBASE-DR optical interface
- Compliant with IEEE 802.3ck-2022: 8x100GAUI-1 C2M electrical interface
- Compliant with QSFP-DD MSA HW Rev 7.0 type 2B with Dual MPO-12 connector
- Compliant with CMIS Rev 5.0
- Case operating temperature 0°C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

Applications

- 800G Ethernet
- Data Centres

Description

The 800GBASE 2xDR4/DR8 QSFP-DD optical transceiver module is designed for 800GBASE Ethernet throughput up to 500m link lengths over OS2 single-mode fiber (SMF) using a wavelength of 1310nm via dual MTP/MPO-12 APC connectors. This transceiver is compliant with QSFP- DD MSA HW Rev 7.0, CMIS Rev 5.0, IEEE 802.3cu-2021 and IEEE 802.3ck-2022 standards. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters.

This module has 2x MPO-12 connectors, supports 2x 400G DR4 and 8x 100G DR breakout applications. Featured with low latency, low power, and reliability, the product is suitable for 800G Ethernet, Data Center, high-performance computing networks, enterprise core and distribution layers, and service provider applications.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	TS	-40	85	°C
Supply Voltage	VCC	-0.5	3.6	V
Relative Humidity (non-condensing)	RH	5	95	%
Data Input Voltage Differential	lVDIP-VDINl		1	V
Control Input Voltage	VI	-0.3	VCC+0.5	V
Control Output Current	IO	-20	20	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	TOPR	0		70	ºC
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Instantaneous peak current at hot plug	ICC_IP			6600	mA
Sustained peak current at hot plug	ICC_SP			5446	mA
Maximum Power Dissipation	PD			16.5	W
Maximum Power Dissipation, Low Power Mode	PDLP			2	W
Signalling Speed per Lane	DRL		53.125		GBd
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V
Control Input Voltage Low	VIL	-0.3		VCC*0.3	V
Two Wire Serial Interface Clock Rate				400	kHz
Power Supply Noise 1 kHz - 1 MHz (p-p)				66	mVpp
Operating Distance		2		500	m

Optical Characteristics

Transmitter Optical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Wavelength	λC	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each lane	AOPL	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMAouter),each Lane	TOMA	-0.8		4.2	dBm	
Launch power in OMAouter minus TDECQ, each lane for extinction ratio >= 5 dB for extinction ratio < 5 dB	TOMA-TDECQ	 -2.2 -1.9			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ			3.4	dB	
TDECQ – 10log10(Ceq), each lane	Ceq			3.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF			-15	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter transition time	Tr			17	ps	
RIN15.5OMA	RIN			-136	dB/Hz	
Optical return loss tolerance	ORL			15.5	dB	
Transmitter Reflectance	TR			-26	dB	2

Receiver Optical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Wavelength	λC0	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOPD	5			dBm	
Average Receive Power, each Lane	AOPR	-5.9		4	dBm	
Receive Power (OMAouter), each Lane	OMAR			4.2	dBm	

Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMAouter), each Lane	SOMA			Max(–3.9, SECQ – 5.3)	dBm	3
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS			-1.9	dBm	4
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ		3.4		dB	
SECQ – 10log10(Ceq), lane under test	Ceq			3.4	dB	
OMAouter of each aggressor lane			4.2		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
4. Measured with conformance test signal at TP3 for the BER = 2.4x10(-)(4).

Electrical Characteristics

High Speed Signal-Receiver (Module Output, TP4)

Parameter	Symbol	Min	Typ	Max	Unit
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB				32 80	mV
Differential peak-to-peak output voltage Short mode Long mode				600 845	mV
Eye height	EH	15			mV
Vertical eye closure	VEC			12	dB
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB
Effective return loss	ERL	8.5			dB

Differential termination mismatch				10	%
Transition time		8.5			ps
DC common-mode voltage tolerance		-0.35		2.85	V

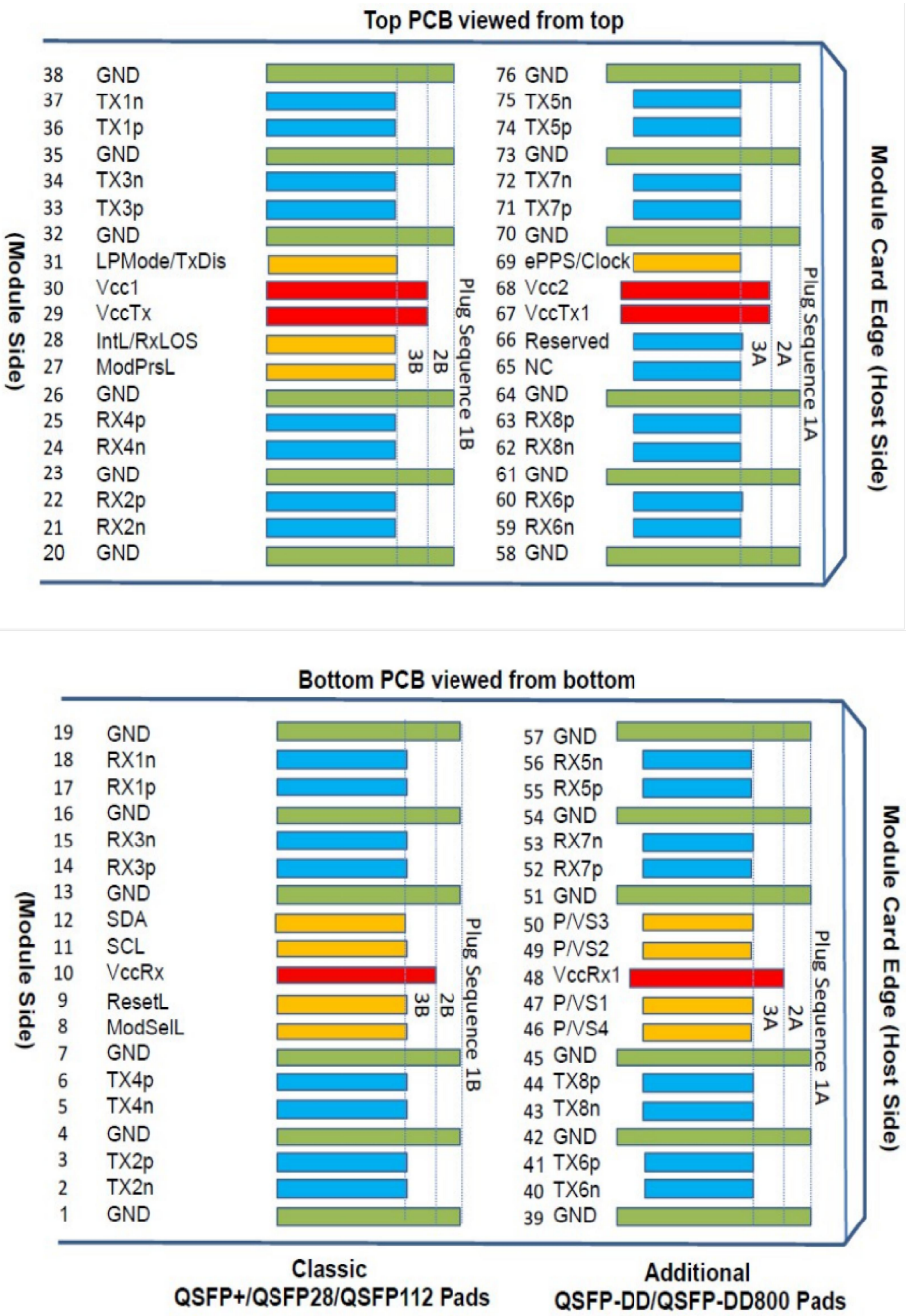
High Speed Signal-Transmitter (Module Input, TP1)

Parameter	Symbol	Min	Typ	Max	Unit
Differential pk-pk input Voltage tolerance (TP1a)		750			mV
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB		32 80			mV
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB
Effective return loss	ERL	8.5			dB
Differential termination mismatch				10	%
Single-ended voltage tolerance range		-0.4		3.3	V
DC common-mode voltage tolerance		-0.35		2.85	V

Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit
Module output SCL and SDA	VOL	0	0.4	V
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V
	VIH	2	VCC+0.3	V
IntL	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V

Pin Description



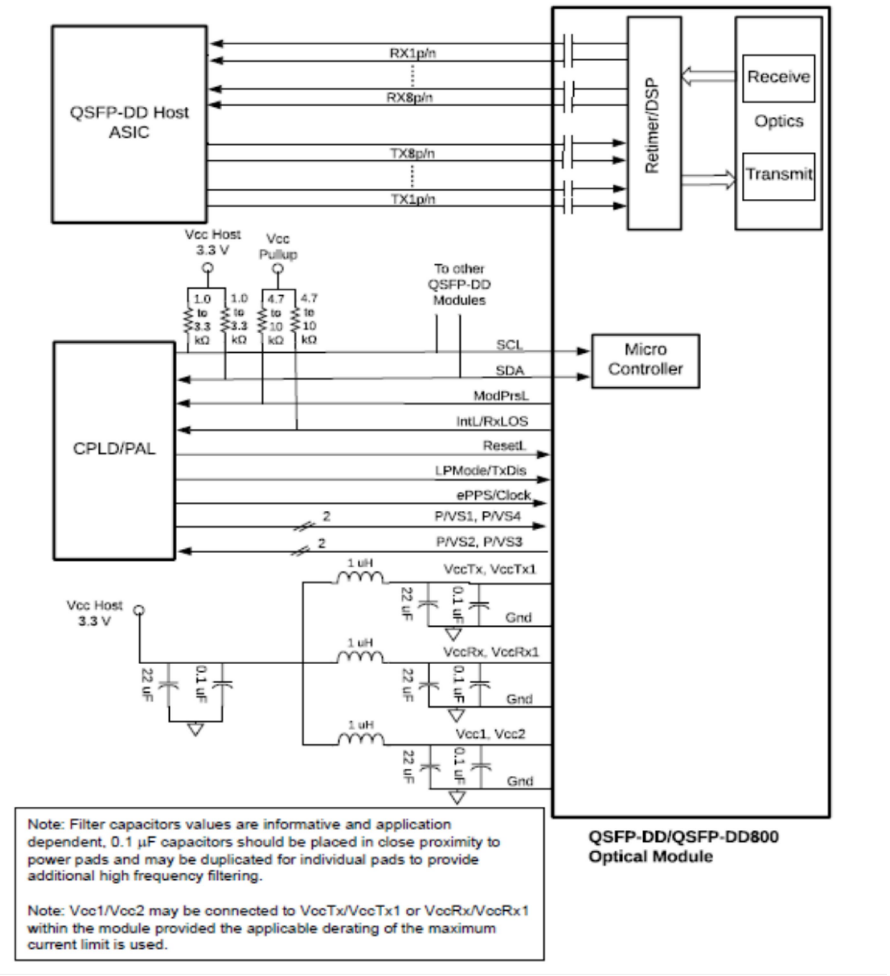
Pad	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3		Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModselL	Module select
9	LVTTL-I	Resetl	Module Reset
10		VccRx	+3.3V Power supply Receiver
11	LVCMOSI/O	SCL	2-wire serial interface clock
12	LVCMOSI/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3P	Receiver Non-Inverted Data output
15	CML-O	Rx3n	Receiver Inverted Data utput
16		GND	
17	CML-O	Rx1p	Receiver Non-Inverted Data output
18	CML-O	Rxln	Receiver Inverted Data output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data output
22	CML-O	Rx2p	Receiver Non-Inverted Data output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data output
25	CML-O	Rx4p	Receiver Non-Inverted Data output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	Intl	Interrupt
29		VccTx	+3.3V Power supply transmitter
30		Vcc1	+3.3V Power supply
31	LVTTL-I	LPMode	Low Power mode
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1P	Transmitter Non-Inverted Data Input
37	CML-I	Txln	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6P	Transmitter Non-Inverted Data Input

42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45		GND	Ground
46	LVCMOS/CML-I	Reserved	For future use
47	LVCMOS/CML-I	Vs1	Module Vendor specific 1
48		VccRx1	3.3v Power supply
49	LVCMOS/CML-O	Vs2	Module Vendor specific 2
50	LVCMOS/CML-O	Vs3	Module Vendor specific 3
51		GND	Ground
52	CML-O	Rx7P	Transmitter Non-Inverted Data Input
53	CML-O	Rx7n	Receiver Inverted Data output
54		GND	Ground
55	CML-O	Rx5p	Transmitter Non-Inverted Data Input
56	CML-O	Rx5n	Receiver Inverted Data utput
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Transmitter Inverted Data Input
60	CML-O	Rx6p	Transmitter Non-Inverted Data Input
61		GND	Ground
62	CML-O	Rx8n	Transmitter Inverted Data Input
63	CML-O	Rx8p	Transmitter Non-Inverted Data Input
64		GND	Ground
65		NC	No Connect
66		Reserved	For future use
67		VccTx1	
68		Vcc2	
69	LVCMO S-I	ePPs	
70		GND	Ground
71	CML-I	Tx7P	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input
75	CML-I	Tx5n	
76		GND	Ground

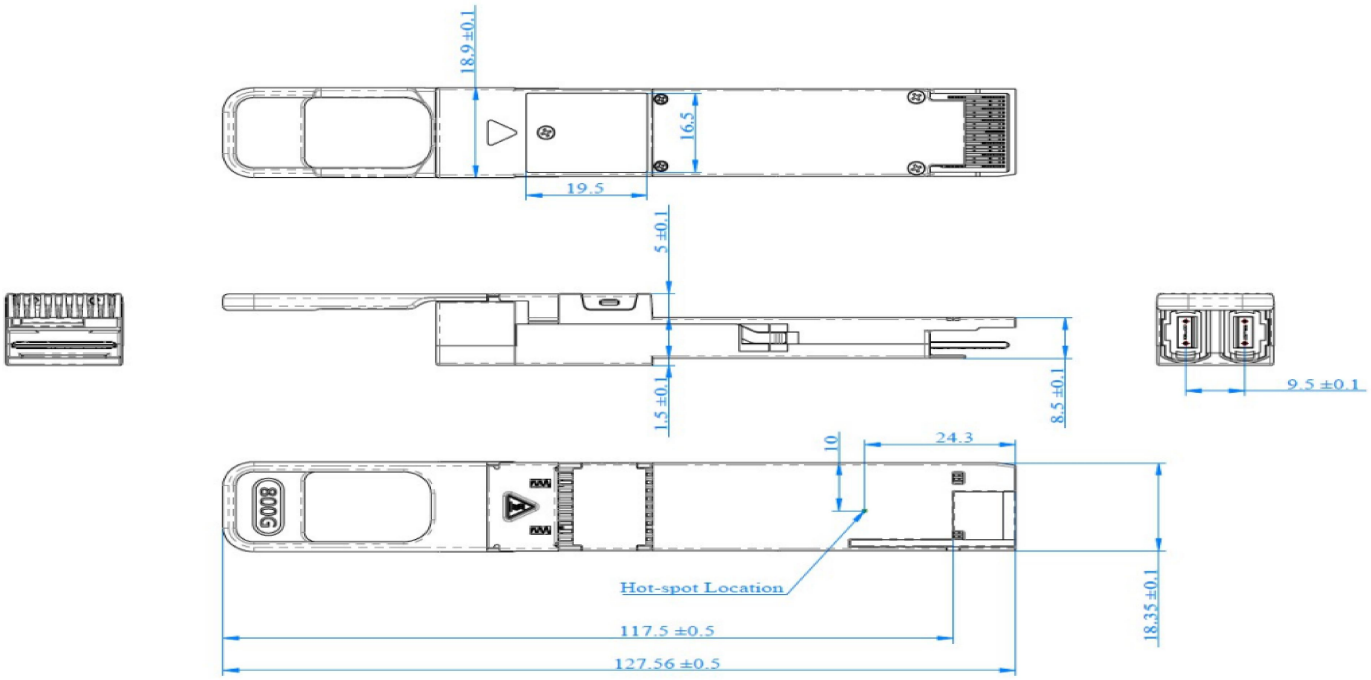
Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	3.135 to 3.465	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 120	10%	mA	Internal
Tx Output Power (Each Lane)	-2.9 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-5.9 to +4	±3	dB	Internal

Recommended Host Board Schematic



Package Outline



Ordering information

Part Number	Product Description
LQD-DM31800-DR8C	800Gbps, QSFP-DD, 1310nm, DR8,Dual MPO-12/APC SMF 500m, 0° C~+70°C, with DDM