LQD-CW800-2FR4C

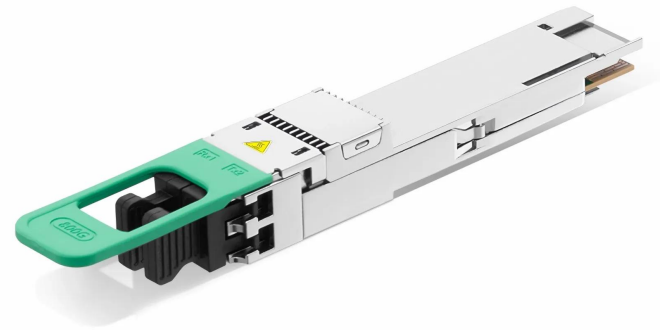
800GBASE-2FR4 QSFP-DD 1310nm 2km
Dual Duplex LC DOM Transceiver

Product Features

- Compliant with IEEE 802.3cu-2021: 2x400GBASE-FR4 optical interface
- Compliant with IEEE P802.3ck D3.0 2x400GAUI-4 C2M electrical interface
- Compliant with QSFP-DD800 MSA HW Rev 6.01 with dual LC connector
- Compliant with CMIS Rev 5.0
- Two wire serial Interface with digital diagnostic monitoring
- Case Temperature Range: 0 ~ +70℃
- Class 1 Laser
- Built-in Broadcom 7nm DSP Chip
- Maximum Power Consumption 17W
- Dual-interface design enables flexible 2x 400G or 8x 100G Breakout networking

Applications

- 800G Ethernet
- Data Center
- Breakout 2x 400G FR4 or 8x 100G FR



Descriptions

The LQD-CW800-2FR4C Optical Transceiver Module is designed for 800GBASE Ethernet throughput up to 2km over eight pairs of singlemode fiber (SMF) with Dual Duplex LC/UPC connectors. This transceiver is compliant with IEEE P802.3ck, IEEE 802.3cu, QSFP- DD MSA. This module has 2 duplex LC connectors, enabling 2 physically distinct 400G FR4 links from each 800G transceiver without the need for optical breakout cables. Also, it can be capable of operation at 1/2 speed (with each electrical lane running at 50G PAM-4 instead of 100G PAM-4). It's suitable for 800G Ethernet, Data Center, Breakout 2x 400G FR4/200G FR4 or 8x 100G FR applications.

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	TSTG	-40	+85	°C
Supply Voltage	VCC	-0.5	3.6	V
Relative Humidity (Non-condensing)	RH	5	95	%
Data Input Voltage Differential	lVDIP-VDINl		1	V
Control Input Voltage	VI	-0.3	VCC+0.5	V
Control Output Current	IO	-20	20	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating Case Temperature	TOPR	0		70	℃
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Instantaneous Peak Current at Hot Plug	ICC_IP			7200	mA
Sustained peak Current at Hot Plug	ICC_SP			5940	mA
Maximum Power Dissipation	PD			17	W
Maximum Power Dissipation, Low Power Mode	PDLP			2.5	W
Signalling Speed per Lane	DRL		53.125		GBd
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V
Control Input Voltage Low	VIL	-0.3		VCC*0.3	V
Two Wire Serial Interface Clock Rate				400	kHz
Power Supply Noise 1kHz -1MHz (p-p)				66	mVpp
Operating Distance		2		2000	m

Optical Characteristics

Transmitter Optical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Wavelength L0, L4	λC0, λC4	1264.5	1271	1277.5	nm	
Wavelength L 1, L5	λC1, λC5	1284.5	1291	1297.5	nm	
Wavelength L2, L6	λC2, λC6	1304.5	1311	1317.5	nm	
Wavelength L3, L7	λC3, λC7	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	AOPT			10.4	dBm	
Average Launch Power, Each Lane	AOPL	-3.2		4.4	dBm	1
Outer Optical Modulation Amplitude (OMAouter), Each Lane for TDECQ<1.4dB for 1.4dB<=TDECQ<=3.4dB	TOMA	-0.2 –1.6 + TDECQ		3.7	dBm	
Difference in Launch Power between Any Two Lanes (OMAouter)	AOPd			3.9	dB	
Transmitter and Dispersion Eye Closure for PAM4(TDECQ), Each Lane	TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4 (TECQ), Each Lane	TECQ			3.4	dB	
| TDECQ–TECQ |				2.5	dB	
Over/Under-Shoot				22	%	
Transmitter Power Excursion				1.8	dBm	
Average Launch Power of OFF Transmitter, Each Lane	TOFF			-16	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time (max)	Tr			17	ps	
RIN17.1OMA (max)	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			17.1	dB	
Transmitter Reflectance	TR			-26	dB	2

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength

Note 2: Transmitter reflectance is defined looking into the transmitter

Receiver Optical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver						
Wavelength L0, L4	λC0, λC4	1264.5	1271	1277.5	nm	
Wavelength L 1, L5	λC1, λC5	1284.5	1291	1297.5	nm	

Wavelength L2, L6	λC2, λC6	1304.5	1311	1317.5	nm	
Wavelength L3, L7	λC3, λC7	1324.5	1331	1337.5	nm	
Damage Threshold, Each Lane	AOPD	5.4			dBm	
Average Receive Power, Each Lane	AOPR	-7.2		4.4	dBm	
Receive Power (OMAouter), Each Lane	OMAR			3.7	dBm	
Difference in Receive Power between Any Two Lanes (OMAouter) (Max)	AOP g			4.1	dB	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity(OMAouter) for TECQ<1.4 dB for 1.4dB<=TECQ<=3.4dB	SOMA			-4.6 –6 + TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), Each Lane	SRS			-2.6	dBm	1
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test	SECQ		3.4		dB	
OMAouter of Each Aggressor Lane			1.4		dBm	

Note 1: Measured with conformance test signal at TP3 for the BER = 2.4x10-4

Electrical Characteristics (High Speed Signal)

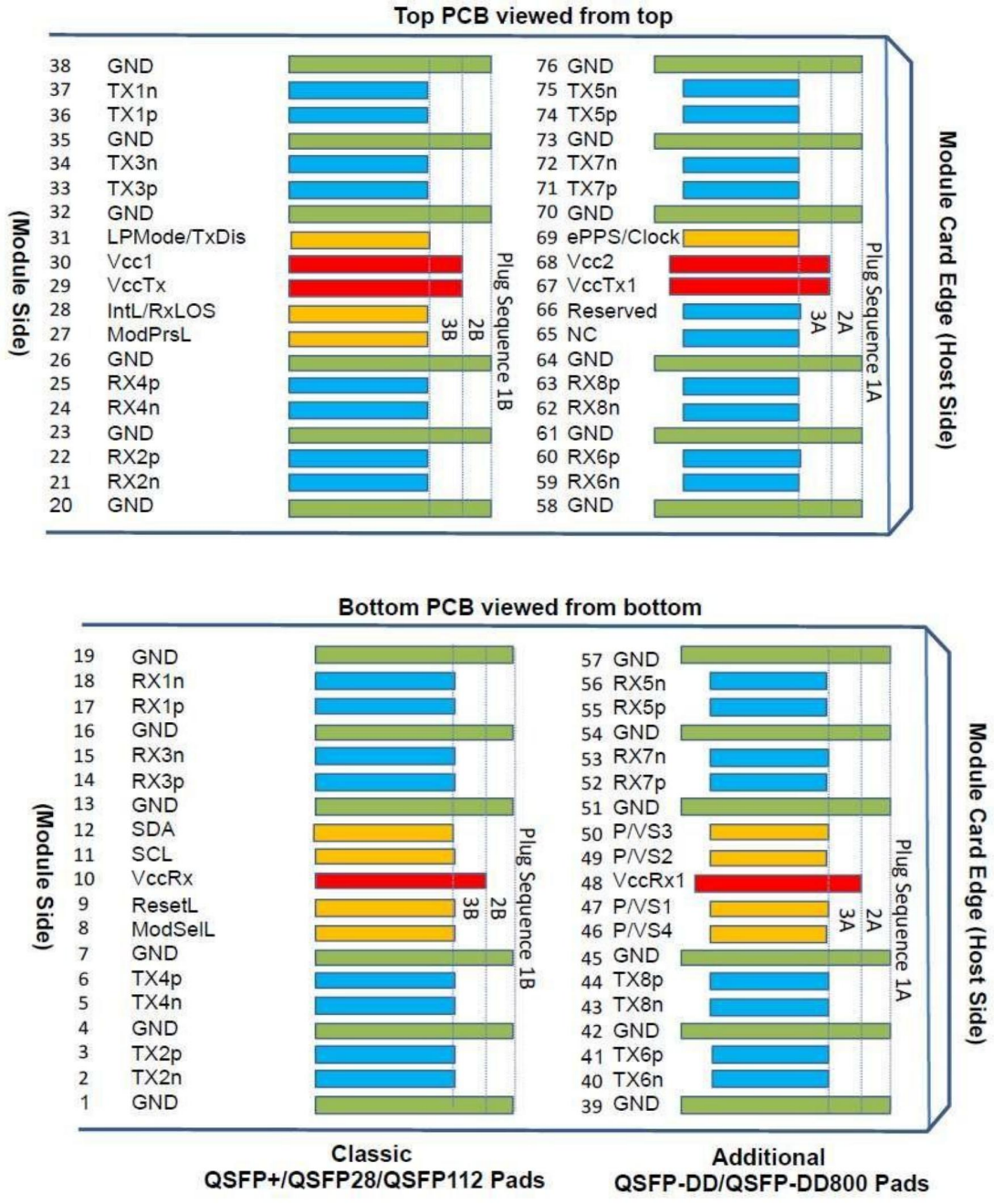
Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Differential Pk-pk Input Voltage Tolerance(TP1a)		750			mV
AC common-mode RMS voltage tolerance (TP1a)		25			mV
Differential-mode to Common-mode Return Loss	RLcd	802.3ck 120G-2			dB
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Single-ended Voltage Tolerancerange		-0.4		3.3	V
DC Common-mode Voltage Tolerance		-0.35		2.85	V
Receiver					
AC common-mode Output Voltage (RMS)				25	mV
Differential Peak-to-peak Output Voltage Short Mode Long Mode				600 845	mV
Eye Height	EH	15			mV
Vertical Eye Closure	VEC			12	dB
Common-mode to Differential-mode Return Loss	RLDc	802.3ck120G-1			dB

Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Transition Time		8.5			ps
DC Common-mode Voltage Tolerance		-0.35		2.85	V

Electrical Characteristics (Low Speed Control and Sense Signals)

Parameter	Symbol	Min.	Max.	Unit
Module Output SCL and SDA	VOL	0	0.4	V
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V
InitMode, Reset Land ModSelL	VIL	-0.3	0.8	V
	VIH	2	VCC+0.3	V
IntL	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V

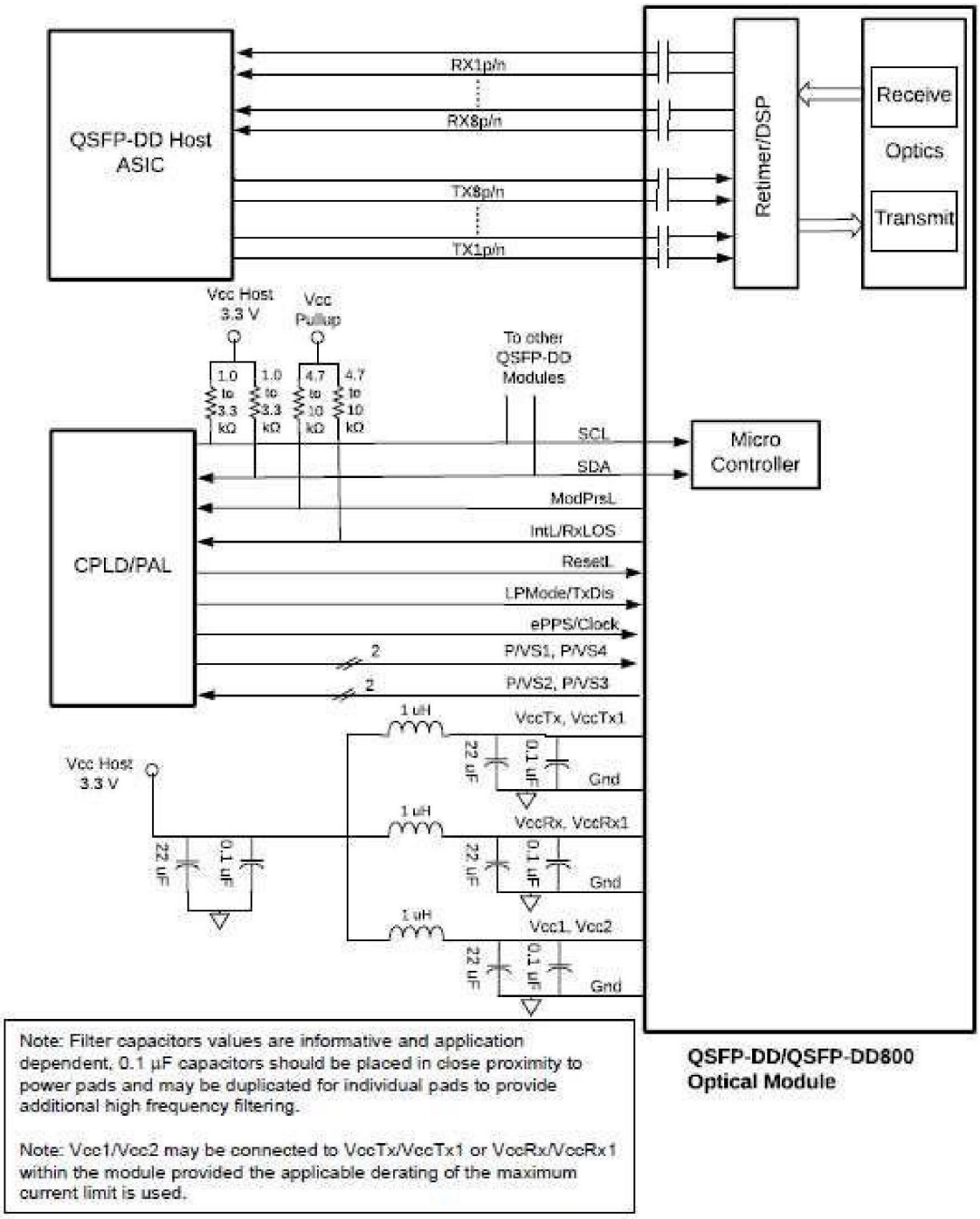
QSFP-DD Edge Connector and Pinout Description



Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	TX2n	Transmitted Inverted Data Input
3	CML-I	TX2p	Transmitted Non-Inverted Data Input
4		GND	Ground
5	CML-I	TX4n	Transmitted Inverted Data Input
6	CML-I	TX4p	Transmitted Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSeil	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VccRx	+3.3V Receiver Power Supply
11	LVCMOS-I/O	SCL	TWI Serial Interface Clock
12	LVCMOS-I/O	SDA	TWI Serial Interface Data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	RX 1p	Receiver Non-Inverted Data Output
18	CML-O	RX 1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	RX2n	Receiver Inverted Data Output
22	CML-O	RX2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	RX4n	Receiver Inverted Data Output
25	CML-O	RX4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/RXLOS	Interrupt/Optional RxLOS
29		VCC TX	+3.3V Power Supply Transmitter
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode/TX Dis	Low Power Mode/Optioanl TX Disable
32		GND	Ground
33	CML-I	TX3p	Transmitted Non-Inverted Data Input
34	CML-I	TX3n	Transmitted Inverted Data Input
35		GND	Ground
36	CML-I	Tx 1p	Transmitted Non-Inverted Data Input
37	CML-I	TX 1n	Transmitted Inverted Data Input
38		GND	Ground
39		GND	Ground

40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-inverted Data Input
45		GND	Ground
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1
48		VccRx1	3.3V Power Supply
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-inverted Data Output
64		GND	Ground
65		NC	Not Connected
66		Reserved	
67		VccTx1	3.3V Power Supply
68		Vcc2	3.3V Power Supply
69	LVCMOS-I	ePPS/Clock	1PPS PTP Clock or Reference Clockinput
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

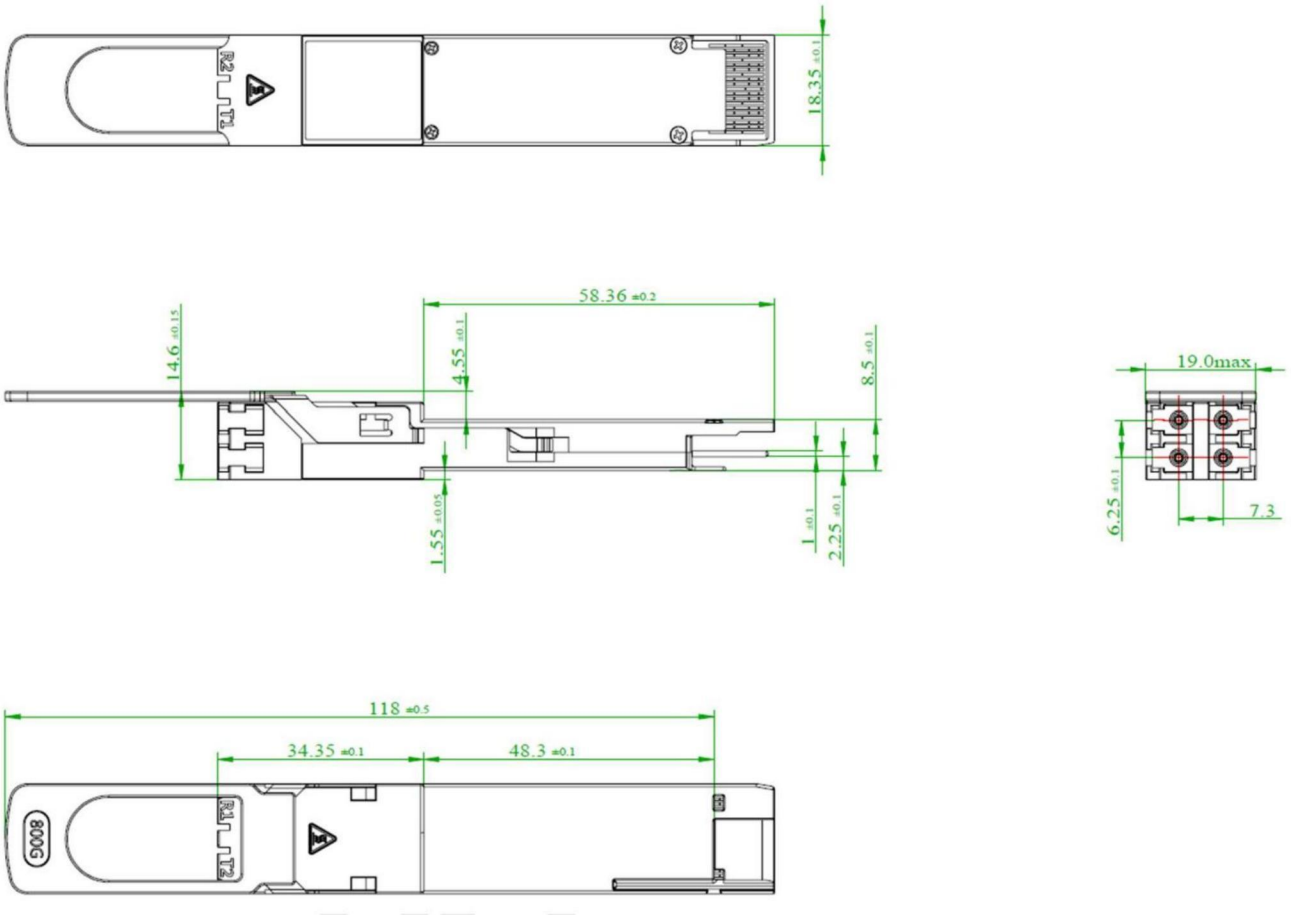
Principle Diagram



Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

Mechanical Specifications(Unit:mm)



Ordering information

Part Number	Product Description
LQD-CW800-2FR4C	800Gbps, QSFP-DD, 2xFR4, CWDM 2km, Dual Duplex LC, with DDM, 0°C~+70°C