LQD-BM85400-SR4C

400G QSFP-DD SR4.2 PAM4
BiDi MPO-12/UPC 850/910nm 100m Transceiver

Product Features

- QSFP-DD MSA
- 8x 53.125Gb/s Electrical Interface(400GAUI-8) Compliant
- Up to 150m OM5 MMF transmission
- MPO-12 Optical Connector
- RoHS-6 Compliant
- Single 3.3 V Power Supply
- Maximum Power Consumption 12W
- Operating Case Temperature: 0°C to 70°C

Applications

- 400G Ethernet
- Data Centre Interconnect

Standards

- QSFP-DD MSA
- IEEE 802.3

Description

The 400GBASE-SR4.2 module, MTP/MPO-12 connector, up to 150m over parallel OM5 multi-mode fiber. It is compliant to IEEE 802.3-2015 protocol and 400GAUI-8/PAM4 standard.

The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 400G ethernet and data center interconnect applications. And it can Support 4× 100G-SR1.2.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Ts	-40	85	°C	
Operating Case Temperature	Top	0	70	°C	
Power Supply Voltage	Vcc	-0.5	3.6	V	
Relative Humidity	RH	0	85	%	
Damage Threshold, each Lane	THd	3.4		dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Case Temperature	Top	0		70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4x10-4		
Post-FEC Bit Error Ratio				1x10-12		1
Link Distance with OM3	D	0.5		70	m	2

Notes:

[1] FEC provided by host system.

[2] FEC required on host system to support maximum distance.

Optical Characteristic

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Center Wavelength	λ 1	844		863	nm	
Center Wavelength	λ2	900		918	nm	
RMS Spectral Width	Δλrms			λ1:0.6 λ2: 0.65	nm	
Average Launch Power, each Lane	PAVG	-6.5		4	dBm	
Optical Modulation Amplitude (OMA), each Lane	POMA	-4.5		3	dBm	1
Launch Power in OMA minus TDECQ, each lane		-5.9			dBm	2
Transmitter Dispersion Penalty ,each lane	TDECQ			4.5	dB	3
TDECQ - 10log10(Ceq), each lane				4.5		4
Extinction Ratio	ER	3.0			dB	
RIN12 OMA				-128	dB/Hz	
Optical Return Loss Tolerance	TOL	12			dB	

Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Encircled Flux		≥86% at 19 µm ≥30% at 4.5 µm				5
Receiver						
Signaling rate, each lane		26.5625+100ppm			Gbps	
Center Wavelength Lane0	λ 1	844		863	nm	
Center Wavelength Lane1	λ2	900		918	nm	
Damage Threshold, each Lane	THd	5			dBm	6
Average Receive Power, each Lane		-8.5		4	dBm	7
Receive Power (OMA), each Lane				3.0	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			Max (-6.6,SECQ –8)Refer toFigure 5	dBm	9
Receiver Reflectance	RR			-12	dB	
Stressed Receiver Sensitivity in OMA, each lane				-3.5	dBm	8

Notes:

[1] Average launch power, each lane (min) is informative and not the principal indicator ofsignal strength. A transmitter with launch power below this value cannot be compliant;however, a value above this does not ensure compliance.

[2] Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed this value.

[3] TDECq is specified and measured as per IEEE802.3.cm Clause 150.8.5.

[4] Ceq is a coefficient defined in IEEE 802.3-2018 Clause 121.8.5.8, which accounts for thereference equalizer noise enhancement.

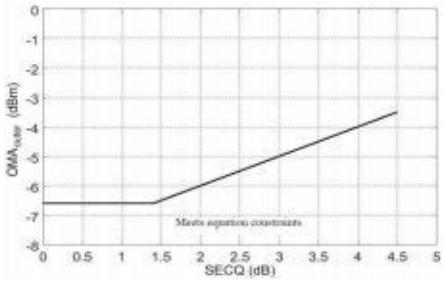
[5] If measured into type A1a.2, or type A1a.3, or type A1a.4, 50 um fibers in accordance withIEC 61280-1-4.

[6] The receiver shall be able to tolerate, without damage, continuous exposure to an opticalinput signal having this average power level on one lane. The receiver does not have tooperate correctly at this input power.

[7] Average receive power, each lane (min) is informative and not the principal indicator ofsignal strength. A received power below this value cannot be compliant; however, a valueabove this does not ensure compliance.

[8] Measured with a conformance test signal at TP3 (see IEEE 802.3 Cl 150) for the BER specified. They are not characteristics of the receiver. The conditions for measuring stressed receiver sensitivity are the following:

Stressed eye closure (SECQ), lane under test	4.5	dB
SECQ – 10log10(Ceq) lane under test (max)	4.5	dBm
OMAouter of each aggressor lane	3.0	dBm



[9] Receiver sensitivity is considered a normative requirement. RX sensitivity is defined for a transmitter with a value of SECQ up to 4.5dB. For transmitter with SECQ different from 4.5dB.

Electrical Specification

Parameter	Test Point	Min	Typ	Max	Unit	Note
Transmitter						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015Equation(83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015Equation(83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver						
Signaling rate, each lane	TP4	26.5625+100ppm			Gbps	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode OutputVoltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output ReturnLoss	TP4	IEEE 802.3 2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015Equation(83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

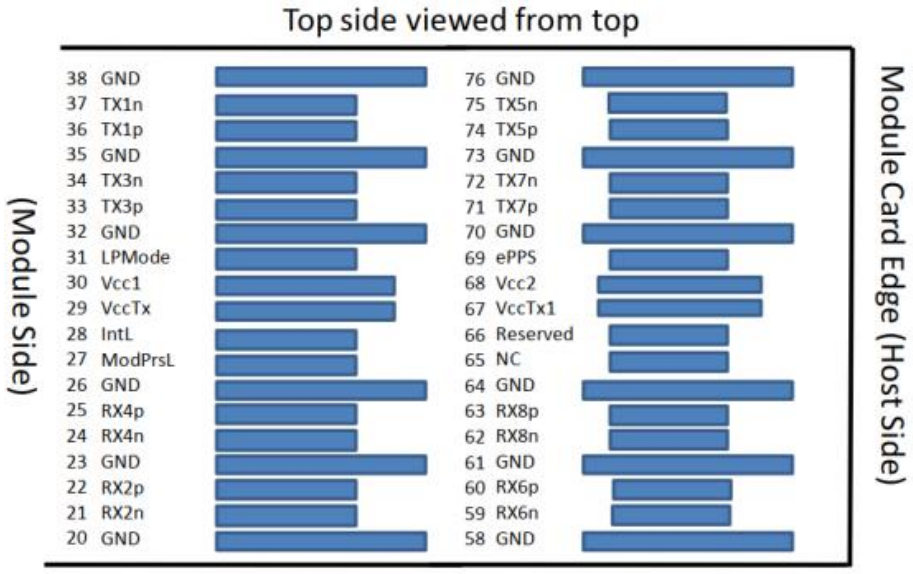
Notes:

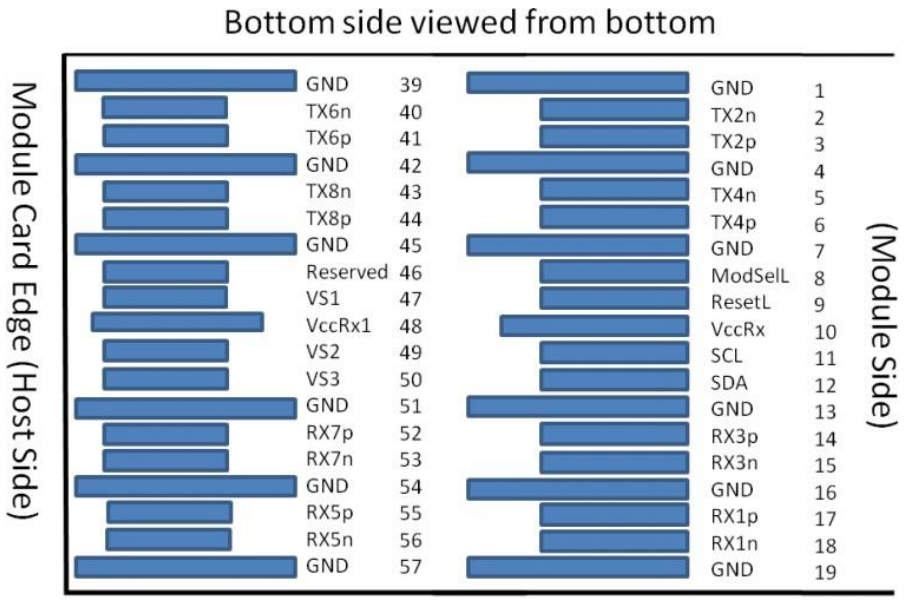
[1] With the exception to IEEE 802.3bs 120E.3.1.2 that the patternis PRBS31Q or scrambled idle.

[2] Meets BER specified in IEEE 802.3bs 120E.1.1.

[3] DC common mode voltage generated by the host. Specificationincludes effects of ground offset voltage.

Pin Description





Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3		Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModselL	Module select	3B	
9	LVTTL-I	ResetI	Module Reset	3B	
10		VccRx	+3.3V Power supply Receiver	2B	2
11	LVCMOSI/0	SCL	2-wire serial interface clock	3B	
12	LVCMOSI/0	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	
14	CML-0	Rx3P	Receiver Non-Inverted Data output	3B	1
15	CML-0	Rx3n	Receiver Inverted Data utput	3B	
16		GND		1B	1
17	CML-0	Rx1p	Receiver Non-Inverted Data output	3B	
18	CML-0	Rxln	Receiver Inverted Data output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-0	Rx2n	Receiver Inverted Data output	3B	
22	CML-0	Rx2p	Receiver Non-Inverted Data output	3B	
23		GND	Ground	1B	1
24	CML-0	Rx4n	Receiver Inverted Data output	3B	
25	CML-0	Rx4p	Receiver Non-Inverted Data output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	Intl	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	1
30		Vcc1	+3.3V Power supply	2B	1
31	LVTTL-I	LPMode	Low Power mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1P	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Txln	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbo1	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6P	Transmitter Non-Inverted Data Input	3A	1
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		Vs1	Module Vendor specific 1	3A	3
48		VccRx1	3.3v Power supply	2A	2
49		Vs2	Module Vendor specific 2	3A	3
50		Vs3	Module Vendor specific 3	3A	3
51		GND	Ground	1A	1
52	CML-0	Rx7P	Transmitter Non-Inverted Data Input	3A	
53	CML-0	Rx7n	Receiver Inverted Data output	3A	
54		GND	Ground	1A	1
55	CML-0	Rx5p	Transmitter Non-Inverted Data Input	3A	
56	CML-0	Rx5n	Receiver Inverted Data utput	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-0	Rx6n	Transmitter Inverted Data Input	3A	
60	CML-0	Rx6p	Transmitter Non-Inverted Data Input	3A	
61		GND	Ground	1A	1
62	CML-0	Rx8n	Transmitter Inverted Data Input	3A	
63	CML-0	Rx8p	Transmitter Non-Inverted Data Input	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1		2A	2
68		Vcc2		2A	2
69		ePPs		3A	3
70		GND	Ground	1A	1
71		Tx7P	Transmitter Non-Inverted Data Input	3A	
72		Tx7n		3A	
73		GND	Ground	1A	1
74		Tx5p	Transmitter Non-Inverted Data Input	3A	
75		Tx5n		3A	
76		GND	Ground	1A	1

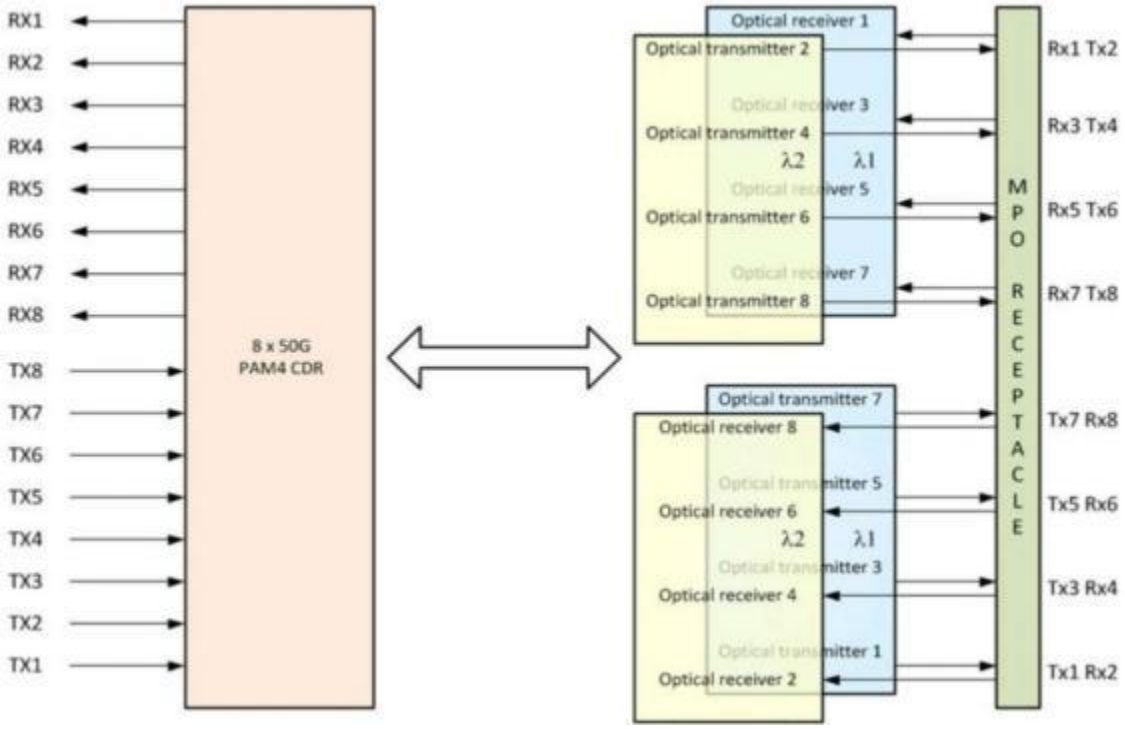
Note 1: QSFP-DD uses comon ground (GND)for all signals and supply (power). A11 are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted, connect these directly to the host board signal-common ground plane .

Note 2: VccRx,VccRx1,Vccl, Vcc2, VccTx and VccTxl shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx,VccRxl, Vccl, Vcc2, VccTx and vccTxl may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

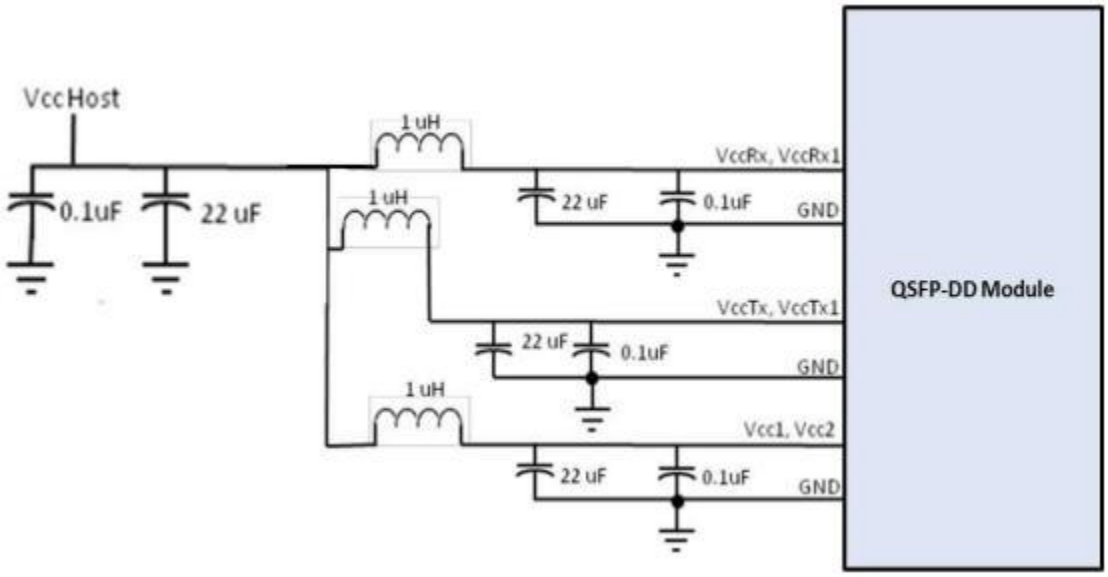
Note 3: All Vendor specific, Reserved, No connect and ePPs (if not used) pins may be terminated with 50 ohms to ground on the host, Pad 65 (No Connect) shall be left unconnected within the module.Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module, The sequence is 1A, 2A, 3A, 1B, 2B, 3B, (see Figure 2 for pad locations)Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B,followed by 3A, 3B

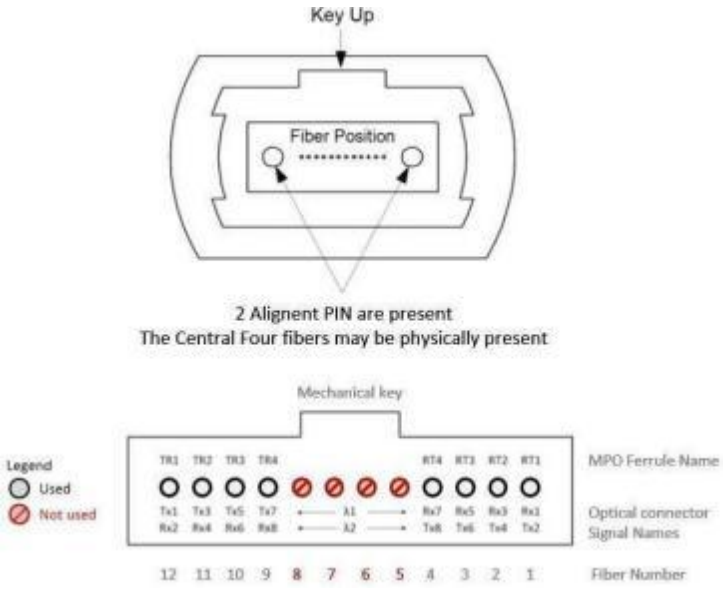
Optical Module Block Diagram



Recommended Power Supply Filter

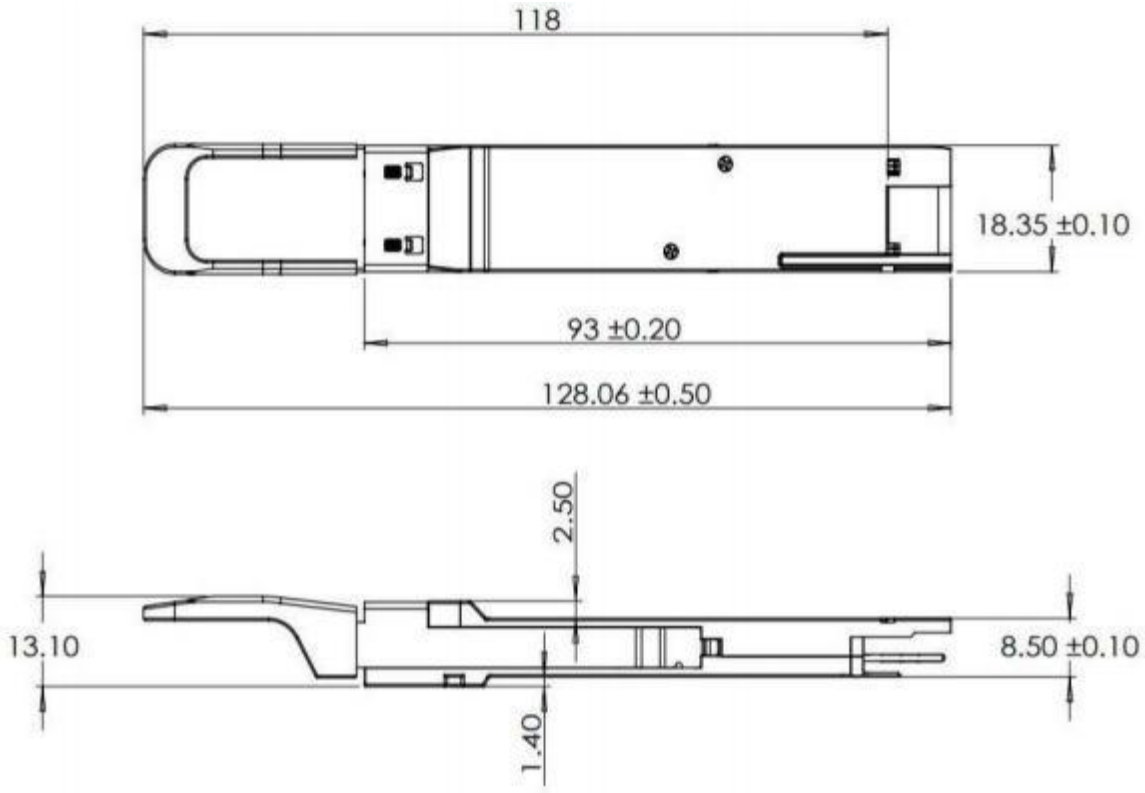


Optical interface



Package Outline

Compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.



Ordering information

Part Number	Product Description
LQD-BM85400-SR4C	QSFP-DD, 400Gbps, MPO-12/UPC, BIDI 850/910nm, SR4, 100m, 0~+70°C, with DDM