LQ-M85100-SR4C

100G QSFP28 SR4 Optical Transceiver

Features

- Compliant with IEEE Std 802.3bm
- Compliant with SFF-8665
- Transmission data rate up to 25.78125 Gbps Data rate per channel
- High Reliability 850nm VCSEL technology
- Electrically hot-pluggable
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃
- Maximum power consumption 2.5W
- Single MPO12 connector
- RoHS complaint

Applications

- 100GBASE-SR4 Ethernet links
- Data centers

General Description

The 100G QSFP28 SR4 is a 4×25Gbps multi mode fiber, hot pluggable optical transceiver. The module integrates four parallel lanes with data rate at 25.78Gbps each lane. It can transmit up to 70 m on fiber OM3 fiber or 100 m on OM4 fiber with FEC.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	T_{STG}	-40	+85	°C
Supply Voltage	V_{CC}	0	4	V
Relative Humidity	RH	5% to 85% non-condensing		

Operating Conditions

Parameter	Symbol	Min	Max	Units
Case Temperature- Operating	T_{CASE}	0	70	°C
Supply Voltage	Vcc	3.14	3.46	V
Power Consumption	P_{DISS}		2.5	W
Link Distance over OM4 Fiber			100	M
Link Distance over OM3 Fiber			70	M

Transmitter Optical Specifications

Transmitter Parameter	Min	Typical	Max	Units
Signaling Rate, each lane		25.78125 ± 100 ppm		Gbps
Center Wavelength Range	840	850	860	nm
Modulation Format		NRZ		
Average launch Power per lane	-8.4		2.4	dBm
RMS spectral width			0.6	nm
Optical Modulation Amplitude , each lane	-6.4		3.0	dBm
Average Launch Power per Lane @ TX Off State			-30.0	dBm
Launch Power in OMA minus TDEC, each Lane	-7.3			dBm
Transmitter and Dispersion Eye Closure, each Lane			4.3	dB
Extinction Ratio	2.0			dB
Optical Return Loss Tolerance			12	dB
Transmitter Eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.3,0.38,0.45,0.35,0.41,0.5}		

Receiver Optical Specifications

Receiver Parameter	Min	Typical	Max	Units
Signaling Rate, each lane		25.78125 ± 100 ppm		Gbps
Lane Wavelength Range	840	850	860	nm
Modulation Format		NRZ		
Damage Threshold	3.4			dBm
Average Receive Power, each lane	-10.3		2.4	dBm
Receiver Power, each lane (OMA)			3.0	dBm
Receiver Reflectance			-12.0	dB
Stressed Receiver Sensitivity (OMA), each lane			-5.2	dBm
Stressed Conditions for Stress Receiver Sensitivity				
Stressed Eye Closure		4.3		dB
stressed Eye J2 Jitter		0.39		UI
stressed Eye J4 Jitter		0.53		UI
OMA of each aggressor lane		3		dBm
Stressed Receiver Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.28,0.5,0.5,0.33,0.33,0.4}		
RX_LOS_Assert Min/Max	-30.0			dBm
RX_LOS_De-Assert Min/Max			-12.0	dBm
RX_LOS_Hysteresis	0.5			dB

QSFP28 Connector and Pinout Description

The electrical interface to the transceiver is a 38 pins edge connector. The 38 pins provide high speed data, low speed monitoring and control signals, I2C communication, power and ground connectivity. The top and bottom views of the connector are provided below, as well as a table outlining the contact numbering, symbol and full description.

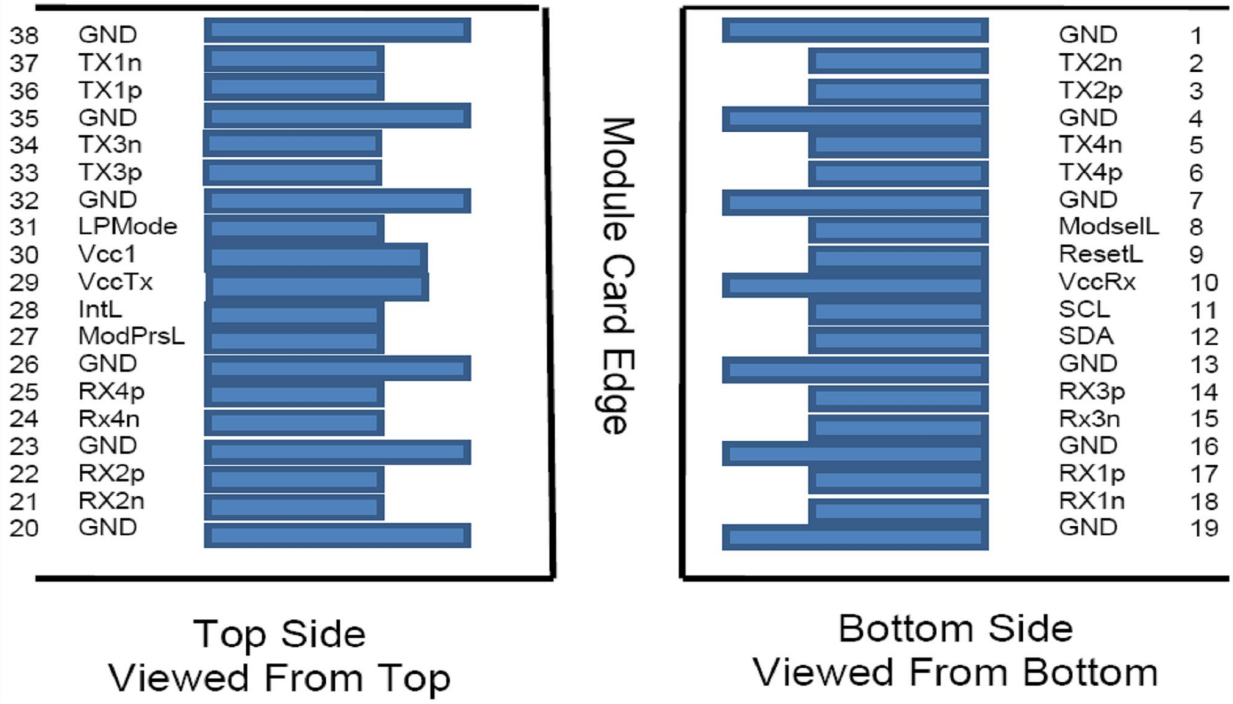

Figure 1. QSFP28-compliant 38-pin connector

QSFP Transceiver Pinout

Pin No.	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1
2	CML-I	TX2n	Transmitted Inverted Data Input	3
3	CML-I	TX2p	Transmitted Non-Inverted Data Input	3
4		GND	Ground	1
5	CML-I	TX4n	Transmitted Inverted Data Input	3
6	CML-I	TX4p	Transmitted Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSeil	Module Select	3
9	LVTTL-I	ResetL	Module Reset	3
10		Vcc Rx	+3.3 VDC Receiver Power Supply	2
11	LVCMOS-I/O	SCL	Serial Clock for I2C Interface	3
12	LVCMOS-I/O	SDA	Serial Data for I2C Interface	3
13		GND	Ground	1
14	CML-O	RX3p	Receiver Non-Inverted Data Output	3
15	CML-O	RX3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	RX1p	Receiver Non-Inverted Data Output	3
18	CML-O	RX1n	Receiver Inverted Data Output	3
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	RX2n	Receiver Inverted Data Output	3
22	CML-O	RX2p	Receiver Non-Inverted Data Output	3
23		GND	Ground	1
24	CML-O	RX4n	Receiver Inverted Data Output	3
25	CML-O	RX4p	Receiver Non-Inverted Data Output	3
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	3
28	LVTTL-O	IntL	Interrupt	3
29		Vcc Tx	+3.3 VDC Transmitter Power Supply	2
30		Vcc1	+3.3 VDC Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	3
32		GND	Ground	1
33	CML-I	TX3p	Transmitted Non-Inverted Data Input	3
34	CML-I	TX3n	Transmitted Inverted Data Input	3
35		GND	Ground	1
36	CML-I	TX1p	Transmitted Non-Inverted Data Input	3
37	CML-I	TX1n	Transmitted Inverted Data Input	3
38		GND	Ground	1

High Speed Electrical Specifications

Transmitter Parameter	Min	Typical	Max	Unit
Signaling rate per lane (range)		25.78125 ± 100 ppm		GBd
AC common-mode output voltage (RMS)			17.5	mV
Differential output voltage			900	mV
Eye width	0.57			UI
Eye height, differential	228			mV
Vertical eye closure			5.5	dB
Differential output return loss	Equation (83E–2)			dB
Common to differential mode conversion return loss	Equation (83E–3)			dB
Differential termination mismatch			10	%
Transition time (20% to 80%)	12			ps
DC common mode voltage	-350		2850	mV
Receiver Parameter	**Min**	**Typical**	**Max**	**Unit**
Signaling rate per lane (range)		25.78125 ± 100 ppm		GBd
AC common-mode output voltage (RMS)			17.5	mV
Differential output voltage			900	mV
Eye width	0.57			UI
Eye height, differential	228			mV
Vertical eye closure			5.5	dB
Differential output return loss	Equation (83E–2)			dB
Common to differential mode conversion return loss	Equation (83E–3)			dB
Differential termination mismatch			10	%
Transition time (20% to 80%)	12			ps

Functional Block Diagram

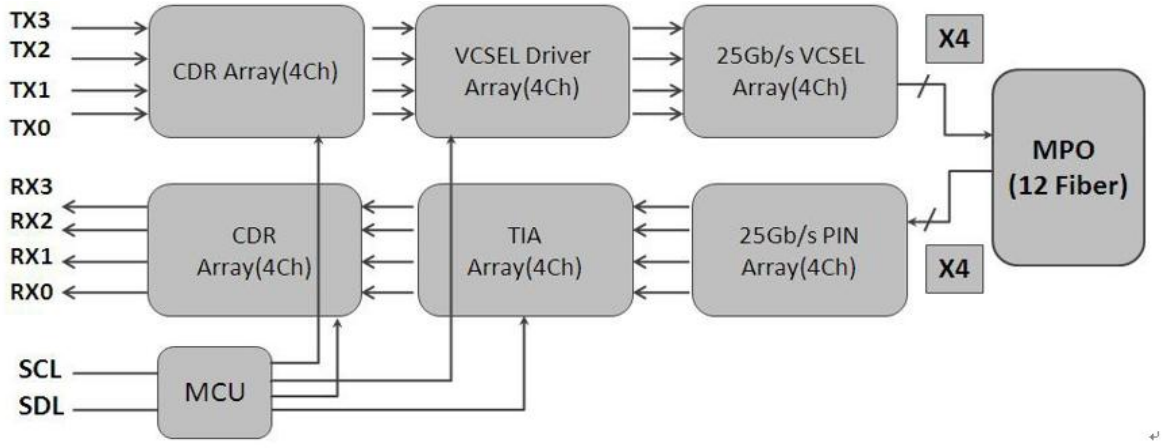

Figure 2. Functional Block Diagram

Mechanical Specifications

Unit：mm

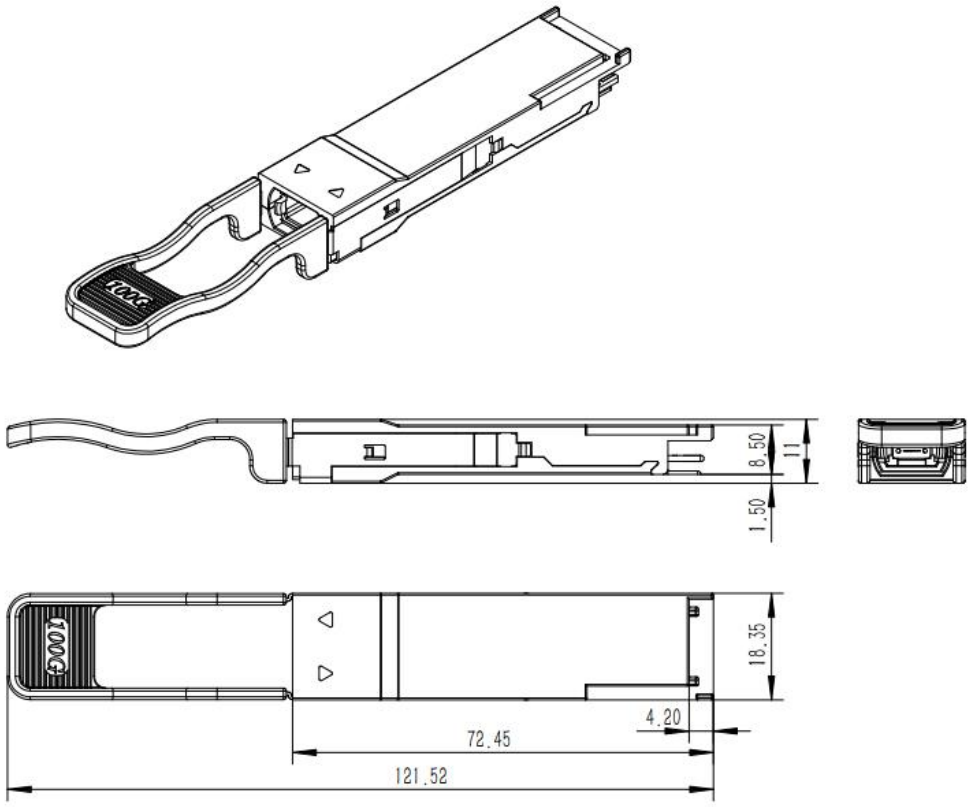

Figure 3. Mechanical Dimensions