LQ-M31400-DR4C

400G QSFP112 DR4 MPO-12/APC Optical Transceiver

Product Features

- Compliant with IEEE Std 802.3ck, IEEE Std 802.3bs
- Compliant with 400Gbase-DR4 optical specifications
- Compliant with QSFP112 MSA Ver 2.0 type2
- Form factor of QSFP112 type2(87.4mm)
- Compliant with CMIS5.0 Management interface specifications
- MPO12 receptacle with APC end face
- 4x106. 25Gb/selectrical interface (400GAUI-4)
- Up to 0.5km transmission on single mode fiber (SMF) with FEC
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃
- Maximum power consumption 10W
- RoHS 2.0 complaint

Applications

- 400G Ethernet
- Data Center Interconnect
- Infiniband Interconnect
- Enterprise Networking

Features

- Compliant to QSFP112 MSA Rev 2.0
- Parallel 4 Optical Lanes
- IEEE 802.3bs 400GBASE-DR4 Specification compliant
- Maximum power consumption 10W

Descriptions

This product is a 400Gb/s QSFP112 optical module designed for 0.5Km optical communication applications. The module converts 4 channels of 100Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s.

On the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 4 channels of 100Gb/s (PAM4) electrical output data.

An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP112 DR4 module receptacle. Host FEC is required to support up to 0.5Km fiber transmission.

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	TSTG	-40	+85	°C
Supply Voltage	VCC	0	4	V
Relative Humidity	RH	10% to 90% non-condensing		

Operating Conditions

Parameter	Symbol	Min	Max	Units
Case Temperature- Operating	TCASE	0	70	°C
Supply Voltage	Vcc	3.14	3.46	V
Power Consumption	PDISS		10	W
Pre-FEC Bit Error Ratio			$2.4x10^{-4}$	
Link Distance			500	M

Optical Characteristics

Transmitter Parameter	Min	Typical	Max	Units	Note
Signaling rate each lane		53.125		GBd	
Lane Wavelength Range	1304.5	1310	1317.5	nm	
Modulation Format			PAM4		
Average Optical Power per lane	-2.9		4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane	-0.8		4.2	dBm	
Average Launch Power per Lane @ TX Off State			-15	dBm	
Launch Power in OMAouter minus TDECQ, each Lane	-2.2			dB	
Transmitter and Dispersion Eye Closure for PAM4, each Lane			3.4	dB	
Extinction Ratio	3.5			dB	
Relative Intensity Noise21.4 (OMA)			- 136	dB/Hz	
Side-Mode Suppression Ration (SMSR)	30			dB	
Optical Return Loss Tolerance			21.4	dB	
Transmitter Reflectance			-26	dB	

Receiver Parameter	Min	Typical	Max	Units	Note
Signaling rate each lane		53.125		GBd	
Lane Wavelength Range	1304.5	1310	1317.5	nm	
Modulation Format		PAM4			
Damage Threshold	5			dBm	
Average Receive Power, each lane	-5.9		4	dBm	
Receiver Power, each lane (OMA)			4.2	dBm	
Receiver Reflectance			-26	dB	
Receiver Sensitivity each lane (OMAouter)			Equation	dBm	1
Stressed Receiver Sensitivity (OMAouter), each			-1.9	dBm	
Stressed Conditions for Stress Receiver Sensitivity					
Stressed Eye Closure for PAM4 (SECQ), Lane under Test		3.4		dB	
OMAouter of each Aggressor Lane		4.2		dBm	

Note: 1.Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation: RS=max (-3.9, -SECQ5.3), where RS is the receiver sensitivity, and SECQ is theSECQ of the transmitter used to measure the receiver sensitivity.

Receiver Thresholds for Loss of Signal (LOS)

Parameter	Min	Typical	Max	Unit	Notes
RX_LOS_Assert Min/Max	-15.0			dBm	
RX_LOS_De-Assert Min/Max			-8.9	dBm	
RX_LOS_Hysteresis		1.5		dB	

Digital Diagnostic Monitoring Specifications

Parameters	Unit	Specification
Temperature Monitor absolute error	°C	±3
Supply Voltage Monitor absolute error	%	±5
I_bias Monitor absolute error	%	±10
Received Power (Rx) Monitor absolute error	dB	±3.0
Transmit Power (Tx) Monitor absolute error	dB	±3.0

Low Speed Electrical signal

Parameter	symbol	Min	Max	Units	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for fast mode,20mA for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc	V	

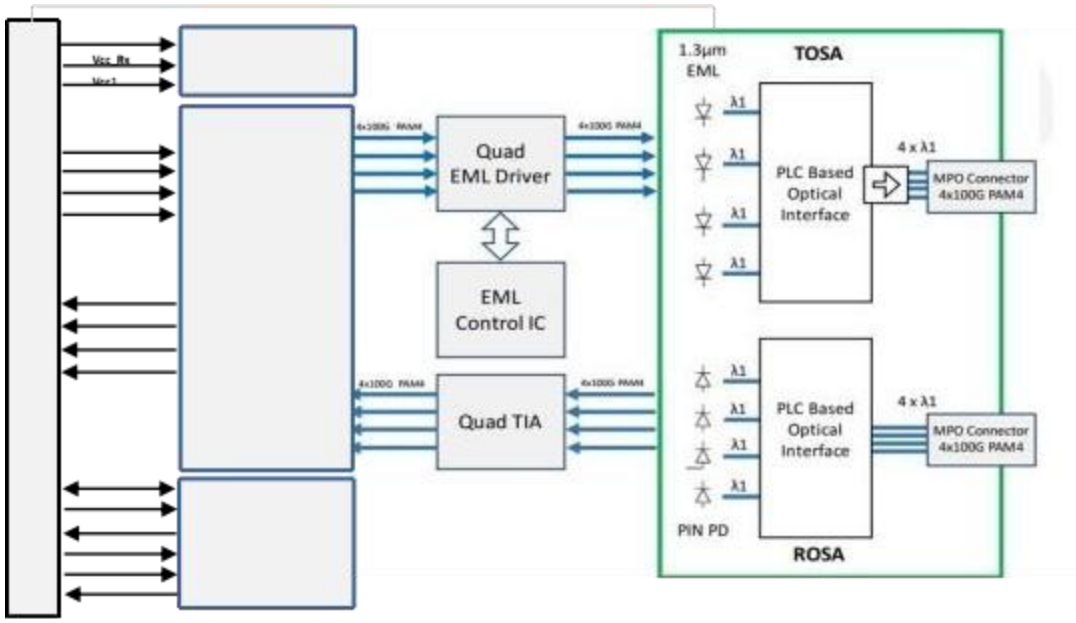
			+0.5		
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus cpacitive load for SCL and SDA	Cb		100	pF	3.0k Ohms Pull up resistor,max
			200	pF	1.6k Ohms Pull up resistor,max
LPMode/TxDis, Reset and ModeSe IL	VIL	-0.3	0.8	V	| Iin| </= 125uA for Vin < Vcc
	VIH	2	Vcc + 0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2 . 0 mA
	VOH	VCC - 0.5	VCC + 0.3	V	10k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	%	IOL=2 . 0 mA
	VOH			dB	ModPrsL can be implemented as a short-circuit to GND on the module

High Speed Electrical signal

Parameter	Min	Typical	Max	Units	Notes
Receiver electrical output characteristics at TP4					
Signaling rate per lane		53.125		GBd	
AC common-mode output voltage(RMS)		-	17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end ESMW (Eye symmetry mask width)		TBD		UI	
Near-end Eye height, differential	24			mV	
Near-end vertical eye closure			7.5	dB	
Far-end ESMW (Eye symmetry mask width)		TBD		UI	
Far-end Eye height, differential	24			mV	
Far-end vertical eye closure			7.5	dB	
Far-end pre-cursor ISI ratio		TBD		%	
Common mode to differential conversion return loss	802.3ck 120G-1			dB	
Effective return loss	TBD			dB	
Differential termination mismatch			10	%	
Transition time (min, 20% to 80%)		TBD		ps	
DC common mode voltage	-350		2850	mV	
Transmitter electrical input characteristics at TP1					
Signaling rate, per lane		53.125		GBd	
Differential pk-pk input voltage tolerance	900			mV	

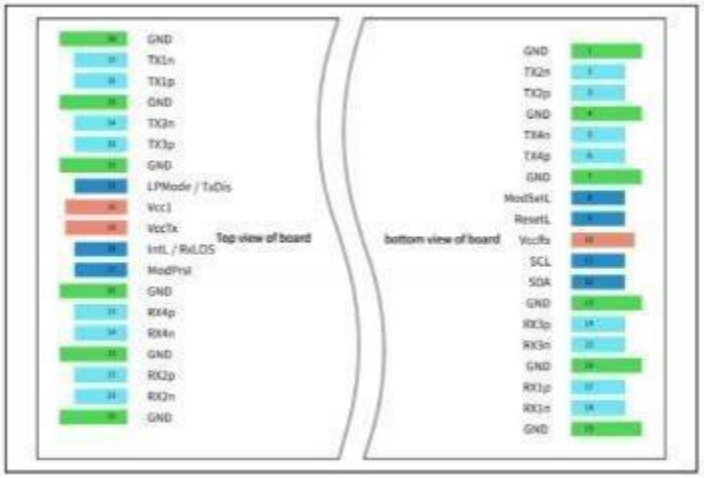
Common-mode to differential return loss	802.3ck Equation(120G-1)				
Effective return loss	TBD				
Differential termination mismatch			10	%	
Module stressed input test	See 120G.3.4.1				
Single-ended voltage tolerance range	-0.4		3.3	V	
DC common-mode voltage	-350		2850	mV	

Module Block Diagram



QSFP112 Edge Connector and Pinout Description

The electrical pinout of the QSFP112 module is shown in Figure below.



QSFP112 module contact assignment

Pin No.	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	TX2n	Transmitted Inverted Data Input	3	
3	CML-I	TX2p	Transmitted Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	TX4n	Transmitted Inverted Data Input	3	
6	CML-I	TX4p	Transmitted Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSeil	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3 VDC Receiver Power Supply	2	2
11	LVCMOS-I/O	SCL	Serial Clock for I2C Interface	3	
12	LVCMOS-I/O	SDA	Serial Data for I2C Interface	3	
13		GND	Ground	1	1
14	CML-O	RX3p	Receiver Non-Inverted Data Output	3	
15	CML-O	RX3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	RX1p	Receiver Non-Inverted Data Output	3	
18	CML-O	RX1n	Receiver Inverted Data Output	3	

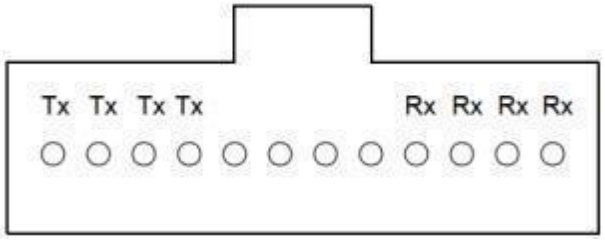
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	RX2n	Receiver Inverted Data Output	3	
22	CML-O	RX2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	RX4n	Receiver Inverted Data Output	3	
25	CML-O	RX4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3	
29		Vcc Tx	+3.3 VDC Transmitter Power Supply	2	2
30		Vcc1	+3.3 VDC Power Supply	2	2
31	LVTTL-I	LPMode/Tx dis	Low Power Mode/optioanl Tx Disable	3	
32		GND	Ground	1	1
33	CML-I	TX3p	Transmitted Non-Inverted Data Input	3	
34	CML-I	TX3n	Transmitted Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	TX1p	Transmitted Non-Inverted Data Input	3	
37	CML-I	TX1n	Transmitted Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

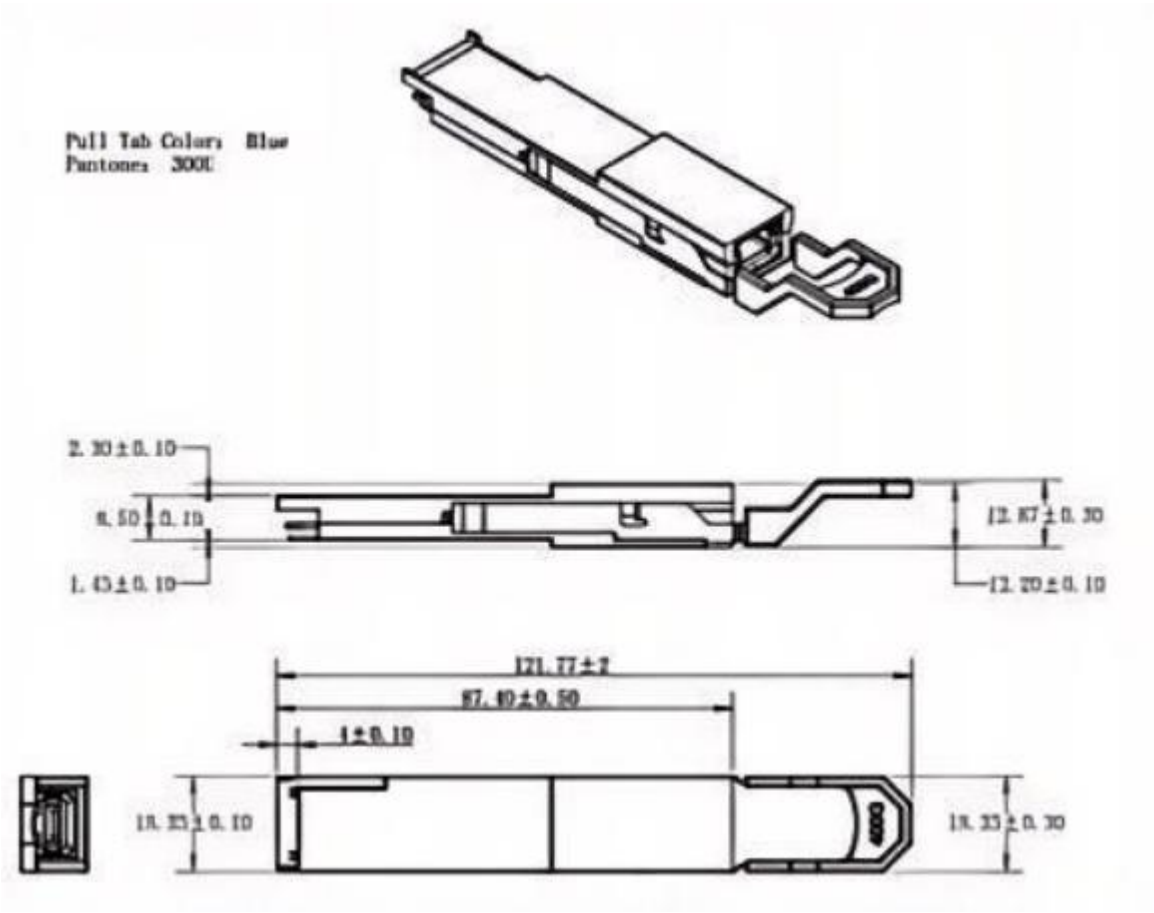
Note 2: Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W) .

Optical interface

The four transmit and four receive optical lanes of the module occupy the positions depicted in Figure when looking into the MPO12 receptacle with the connector keyway feature on top. The interface contains eight active lanes within twelve total positions. The transmit optical lanes occupy the left-most four positions. The receive optical lanes occupy the right-most four positions. The four center positions are unused. To minimize MPO connection induced reflections, a MPO receptacle with 8-degree angled end-face is utilized for this product.



Mechanical Specifications



Ordering information

Part Number	Product Description
LQ-M31400-DR4C	400Gbps, QSFP112, 1310nm, DR4, SMF 500m, 0~70℃, MPO12/APC, with DDM