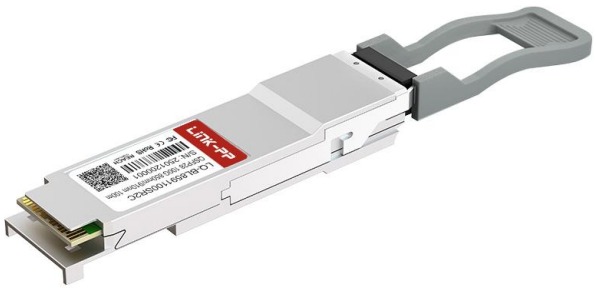
LQ-BL8591100SR2C

100Gb/s 100m QSFP28, Bi-Di, Duplex LC Hot Pluggable,

850/910nm, VCSEL, Multimode

Features

- QSFP28 module form factor
- Support QSFP28 SFF-8436/8636
- 2x53.125Gbps(26.5625GBd) PAM4 parallel optics architecture
- 4x25.78125Gbps NRZ retimed electrical I/O
- Bandwidth density of 100Gbps bi-directional
- 2 channels 850nm/910nm VCSEL and PIN photo detector
- Internal 4:2 Gearbox with KP4 FEC circuits on both receiver and transmitter channels
- Duplex LC connector
- Maximum link length of 100m OM4,70m OM3
- Built-in digital diagnostic functions
- Operating case temperature range: 0 to 70℃
- Single 3.3V power supply
- Low power consumption < 4W
- RoHS compliant (lead free)



Applications

- 100G SR BD applications
- High-speed interconnects within and between switches, routers and transport equipment
- Server-server clusters, super-computing interconnections
- Proprietary backplanes
- Interconnects rack-to-rack, shelf-to-shelf, board-to-board, board-to-optical backplane

Description

The QSFP28-100G-SR-BD optical transceiver is designed for using in 100-Gigabit Ethernet links up to 70m using OM3 and 100m using OM4. It is compliant with the QSFP28 MSA, IEEE802.3cm-2020 and CAUI-4(no FEC)1. Digital diagnostics functions are available via the I2C interface, as specified by the QSFP28 MSA. The module incorporates 2 channels 850nm/910nm VCSEL and PIN photo detector, transmitting and receiving each optically over one simplex LC fiber using bi-directional optics. This results in an aggregate bandwidth of 100Gbps into a duplex LC cable. This module can convert 4 channels of 25Gbps (NRZ) electrical input data to 2 channels of 50Gbps (PAM4) optical signal, and also can convert 2 channels of 50Gbps (PAM4) optical signal to 4 channels of 25Gbps (NRZ) electrical output data. The electrical interface uses a 38-contact edge type connector. This transceiver is a high performance module for short-range duplex data communication and interconnects applications.

Note:

1. KR-FEC is optional, please contact us if necessary.

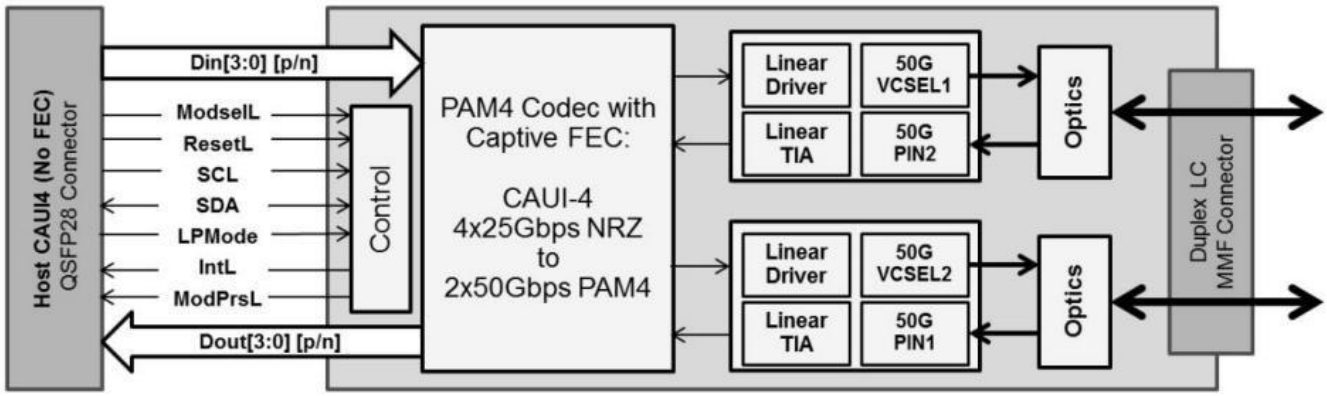


Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Ts	-20	85	℃
Case Operating Temperature	Tc	0	70	℃
Humidity (non-condensing)	Rh	5	85	%

Recommended Operating Environment

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tc	0	-	70	℃
Signal Rate per Electrical Channel (4 x 25G)		-	25.78125	-	Gbps
Signal Rate per Optical Channel (2 x 50G)		-	53.125	-	Gbps
Humidity	Rh	5	-	85	%
Power Dissipation	Pm	-	-	4	W
Fiber Length for OM3		-	-	70	m
Fiber Length for OM3		-	-	100	m

Electrical Characteristics (TOP = 0 to 70 °C, VCC = 3.13 to 3.47 Volts)

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Zin	90	100	110	ohm
Differential Output Impedance	Zout	90	100	110	ohm
Differential Input Voltage Amplitude1	ΔVin	-	-	1200	mVp-p
Differential Output Voltage Amplitude2	ΔVout	-	-	1200	mVp-p

Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.

2. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Parameters(TOP = 0 to 70 °C, VCC = 3.0 to 3.6 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Optical Wavelength CH1	λ1	844	850	863	nm	
Optical Wavelength CH2	λ2	900	910	918	nm	
Average launch power	Pavg	-6.2	-	4	dBm	
Optical Modulation Amplitude(OMA outer)	OMA	-4.2	-	3	dBm	
Transmitter and dispersion eye closure(TDEC)	TDEC	-	-	4.5	dB	
Extinction Ratio	ER	3	-	-	dB	1
Average launch power of OFF transmitter		-	-	-30	dBm	
Receiver						
Optical Center Wavelength CH1	λ	844	850	863	nm	
Optical Center Wavelength CH2	λ	832	850	868	nm	
Receiver Sensitivity per Channel	R	900	910	918	dBm	
Maximum Input Power	PMAX	-	-	(-6.6,-3.5)	dBm	
Damage Threshold	PMin	-8.2	-	4		
Receiver Reflectance	Rrx	-	-	-12	dB	
LOS De-Assert	LOSD	-	-11	-	dBm	
LOS Assert	LOSA	-	-9	-	dBm	
LOS Hysteresis	LOSH	0.5	-	-	dB	

Note:

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FECs

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode =Vih) until

				module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	µs	toff_IntL 500 µs Time from clear on read3 operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
Mask De-assert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	µs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	µs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power consumption enters lower Power Level
Power over-ride or Power-set De-assert Time	Toff down	300	ms	Time from Down bit cleared4 until the module is fully functional3

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction

Pin Assignment

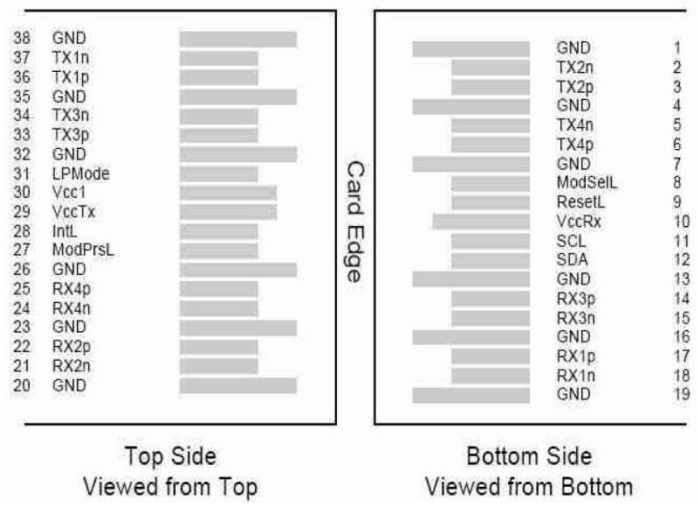


Diagram of Host Board Connector Block Pin Numbers and Name

Pin Description

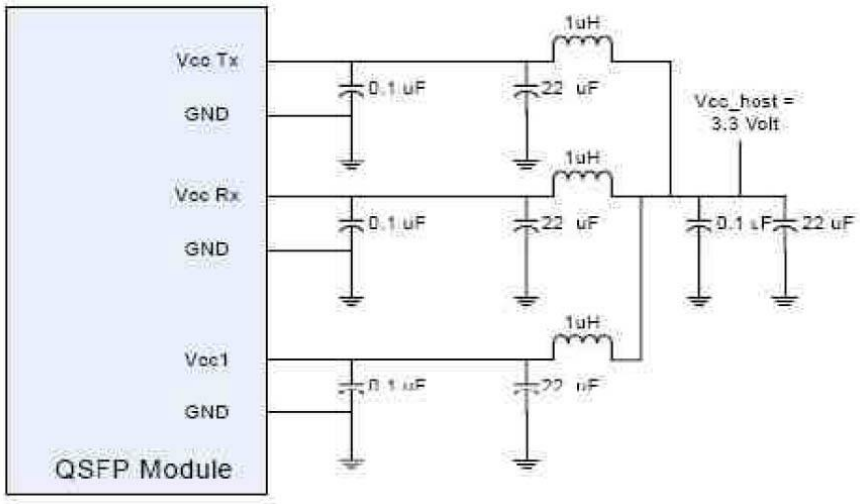
Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1

17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

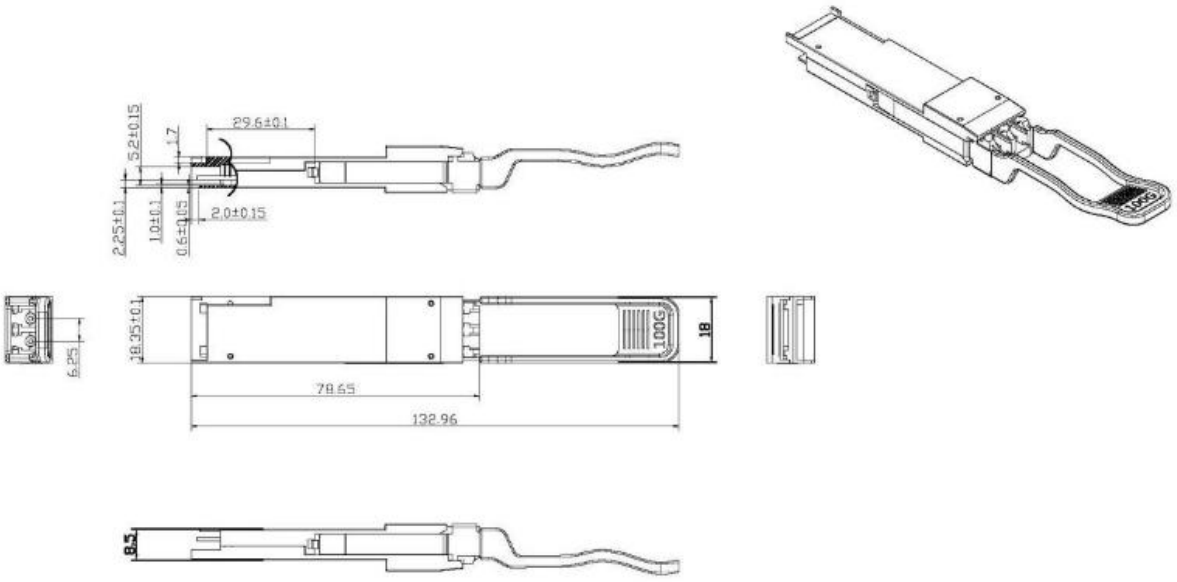
Notes:

1. GND is the symbol for single and supply(power) common for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

Recommended Circuit



Mechanical Dimensions



Ordering information

Part Number	Product Description
LQ-BL8591100SR2C	QSFP28 100G BIDI 850/910nm Duplex LC MMF OM3 70m/OM4 100m DDM