LO-M85400B-SR4C

400GBASE-VSR4 OSFP PAM4 850nm 50m MPO-12/APC Finned Top MMF Transceiver

Features

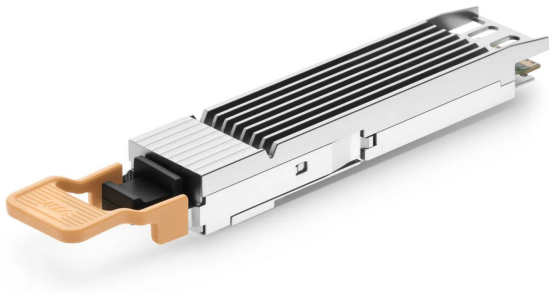
- Built-in Maxlinear DSP Chip
- Maximum Power Consumption 9W
- Tested in Targeted Switches for Superior Performance, Quality, and Reliability
- Case Temperature Range: 0 ~ +70℃
- Class 1 Laser Safety
- Digital Optical Monitoring Capability for Strong Diagnostic Capabilities
- Compliant with OSFP MSA standard
- Compliant with CMIS Rev 5.2
- Compliant with IEEE 802.3 db-400GBASE- VR4 optical interface
- Compliant with IEEE 802.3 bs-400GAUI-8 electrical interface

Applications

- 400G Ethernet

Standards

- OSFP MSA



Description

The LO-M85400B-SR4C Compatible OSFP optical transceiver module is designed for 400GBASE Ethernet throughput up to 50m link lengths over OM4 multimode fiber (MMF) using a wavelength of 850nm via MTP/MPO-12 APC connectors. This transceiver is compliant with CMIS 5.2, IEEE 802.3bs, IEEE 802.3db and OSFP MSA standards. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters.

It is the ideal solution for supercomputing, seamlessly integrating into computing and storage infrastructure to ensure efficient high- performance interconnectivity.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature Range	TSTG	-40		85	℃	
Supply Voltage	VCC	-0.5		3.6	V	
Relative Humidity (Non-condensing)	RH	5		95	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature	Top	0		70	℃	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Link Distance with OM4/OM5	D1	2		50		
Link Distance with OM3	D2	2		30		

Optical Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Wavelength	λ	844	850	863	nm	
RMS Spectral Width				0.6	nm	
Average Launch Power, each Lane	PAVG	-4.6		4	dBm	
Outer Optical Modulation Amplitude (OMAouter), Each Lane (Max)				3.5	dBm	
Outer Optical Modulation Amplitude (OMAouter), Each Lane(min)	POMA	-2.6 - 4.4+max(TECQ,TDECQ)			dBm	
Transmitter and Dispersion Eye Closure for	TDECQ			4.4	dB	
Extinction Ratio, Each Lane	ER	2.5			dB	
Average Launch Power of OFF Transmitter,	Poff			-30	dBm	
Optical Return Loss Tolerance				14	dB	
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Center Wavelength	λ	842		948	nm	
Damage Threshold, each Lane	THd	5			dBm	
Average Receive Power, each Lane		-6.4		4	dBm	
Receive Power (OMA outer), each Lane				3.5	dBm	
Receiver Reflectance	RR			-15	dB	
Receiver Sensitivity (OMAouter),each Lane	SEN			Max(-4.6,-6.4 +TECQ)	dBm	

Stressed Receiver Sensitivity(OMAouter), each Lane	SRS			-2.0	dBm	
RX_LOS_Assert	LOSA	-18.5			dBm	
RX_LOS_De-Assert	LOSD			-5	dBm	
RX_LOS_Hysteresis	Hys	0.5			dBm	
RIN17.1OMA	RIN			-136	dB/Hz	

Electrical Characteristics

Parameter	TestPoint	Min.	Typ.	Max.	Unit	Note
Input Impedance	Zin	90	100	110	W	
Output Impedance	Zout	90	100	110	W	
Input Data Amplitude	Vpp	400		900	mV	
Output Data Amplitude	Vpp			900	mV	
Data Rate, Each Lane	DR		26.5625		GBd	
Input Logic High	VIH	2.0		Vcc+0.3	V	
Input Logic Low	VIL	0		0.8	V	
Output Logic High	VOH	Vcc- 0.4		Vcc+0.3	V	
Output Logic Low	VOL	0		0.4	V	
SDA and SCL Speed	I2C			400	KHz	
SDA and SCL Capacitance	Ci			14	pF	

Pin Map and Description

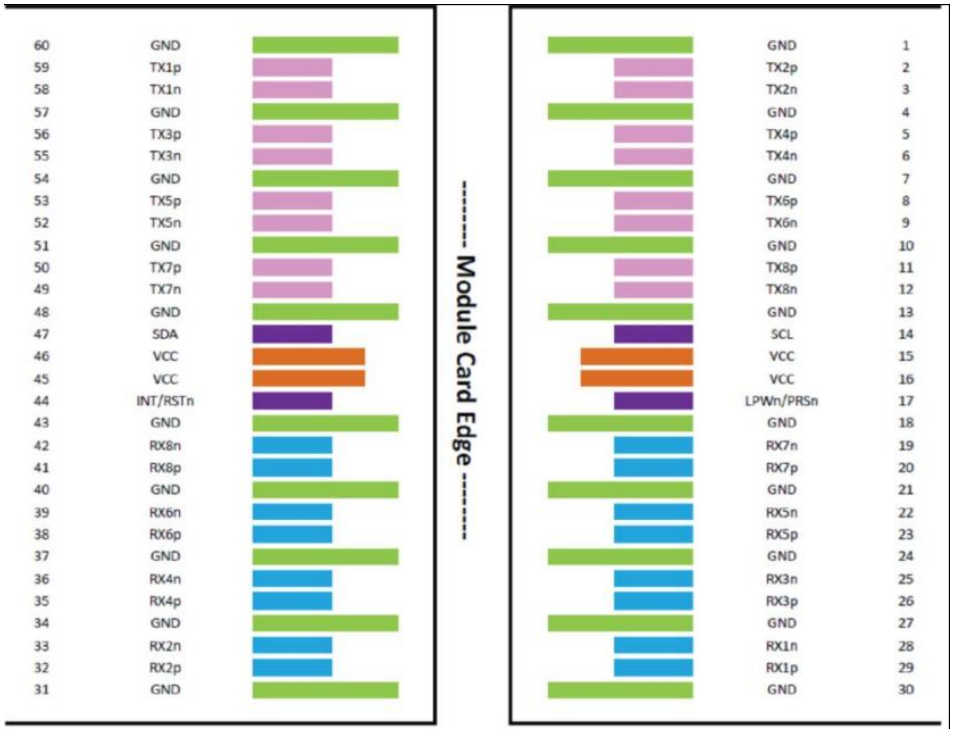


Figure 1. MSA Compliant Connector

Pin#	Symbol	Description	Logic	Direction	Plug
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1

19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

Principle Diagram

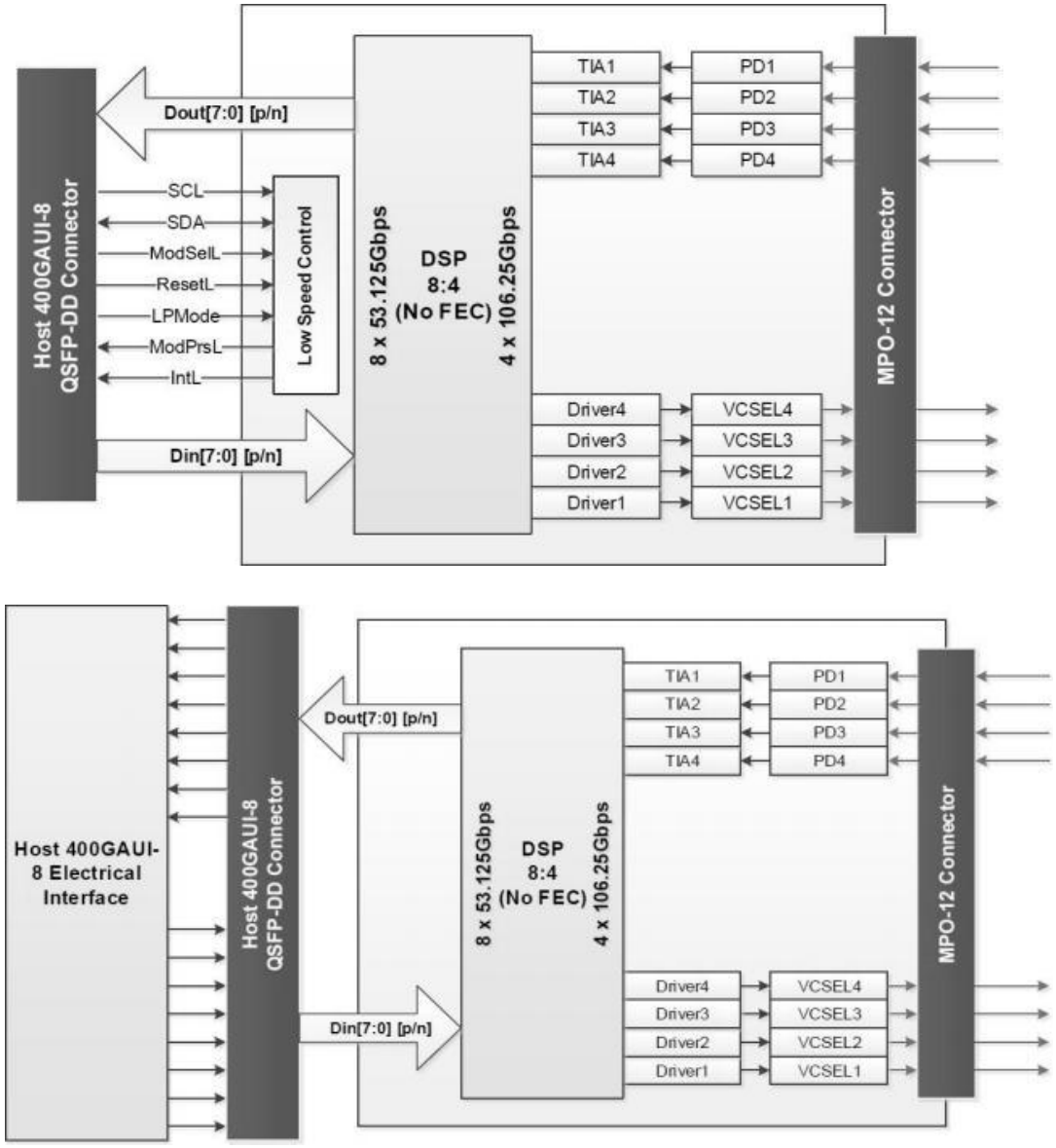


Figure 2.Application Reference Diagram

Optical Interface

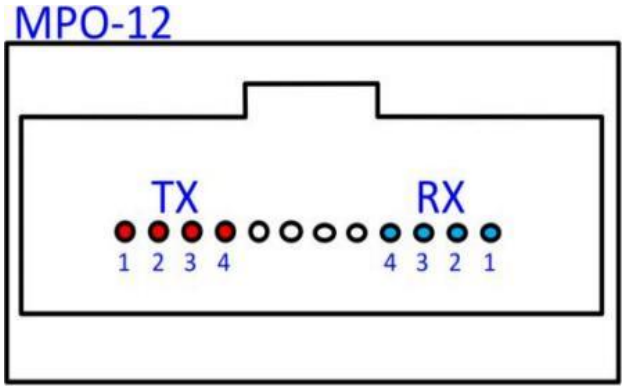


Figure 3. Optical Media Dependent Interface port assignments

Mechanical Drawing

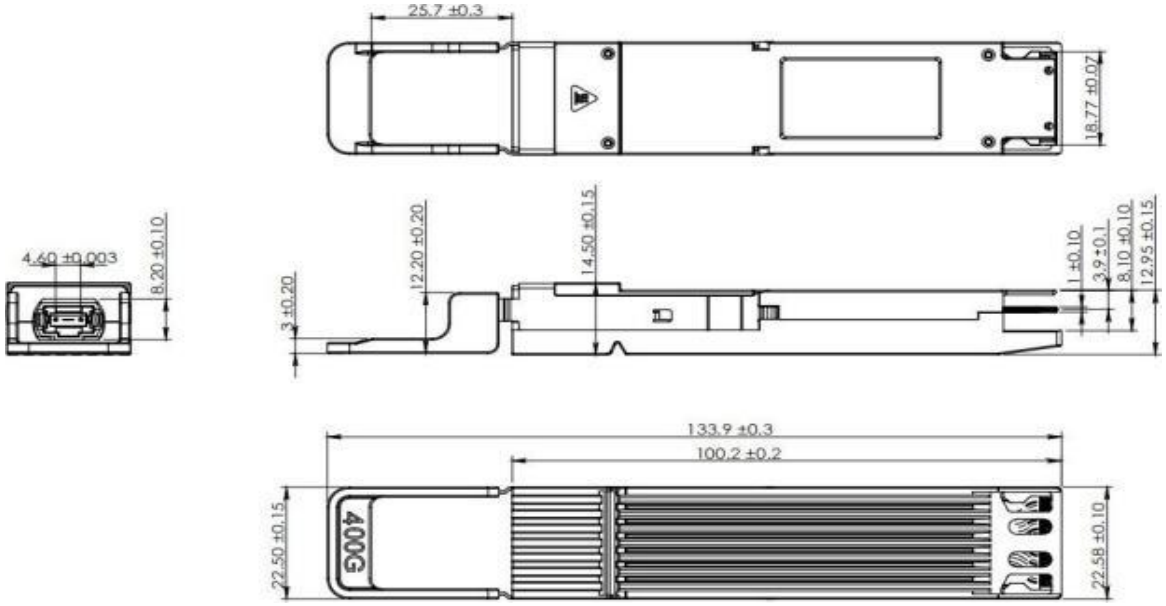


Figure 5. Mechanical Outline

Ordering information

Part Number	Product Description
LO-M85400B-SR4C	OSFP 400G, SR4, MPO-12/APC interface, Finned Top, 850nm, up to 50m, 0° C~+70° C