

LO-M85400A-SR4C

400GBASE-SR4 OSFP PAM4 850nm 50m MTP/MPO Flat Top MMF Transceiver

Features

- OSFP MSA
- Up to 106.25Gbps Data Rate Per Channel by PAM4 Modulation
- Up to 50m OM4 MMF transmission
- MTP/MPO-12 (APC) Optical Connector
- CMIS Compliance
- Single 3.3 V Power Supply
- Maximum Power Consumption 8.5W
- Operating Case Temperature: 0°C to 70°C

Applications

- 400G Ethernet
- Infiniband Interconnect

Standards

- OSFP MSA
- IEEE 802.3ck



Description

The 400GBASE-SR4 OSFP module, MTP/MPO-12 connector, up to 50m over parallel OM4 multi-mode fiber. It is compliant with OSFP MSA, IEEE 802.3ck protocol and 400GAUI-4 standards.

The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 400G Ethernet and Infiniband. It also support 1 x 400G point to point connection.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature	Top	0		70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Data Rate, each Lane			53.125		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4x10 ⁻⁴		
Post-FEC Bit Error Ratio				1x10 ⁻¹²		1
Link Distance with OM4	D1	2		50		2
Link Distance with OM3	D2	2		30		2

Notes:

- [1] FEC provided by host system.
- [2] FEC required on host system to support maximum distance.

Optical Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Wavelength	λ	842		948	nm	
RMS Spectral Width				0.65	nm	1
Average Launch Power, each Lane	PAVG	-4.6		4	dBm	
Outer Optical Modulation Amplitude (OMA _{outer}), each Lane	POMA	-2.6(For max(TECQ, TDECQ) ≤ 1.8 dB)-4.4 + max(TECQ, TDECQ) (For 1.8 < max(TECQ, TDECQ) ≤ 4.4 dB)		3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			4.4	dB	
Transmitter Eye Closure for PAM4, each Lane	TECQ			4.4	dB	
Overshoot/Undershoot				29	%	
Transmitter Power Excursion, each Lane				2.3	dBm	
Extinction Ratio		2.5			dB	
Transition Time	Tt			17	ps	
Average Launch Power of OFF Transmitter, each Lane	Poff			-30	dBm	

RIN 14 OMA	RIN			-132	dB/Hz	
Optical Return Loss Tolerance				14	dB	
Encircled Flux		≥ 86% at 19 μm ≤ 30% at 4.5 μm				2
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Center Wavelength	λ	842		948	Nm	
Damage Threshold, each Lane	THd	5			dBm	3
Average Receive Power, each Lane		-6.3		4	dBm	4
Receive Power (OMA outer), each Lane				3.5	dBm	
Receiver Reflectance	RR			-15	dB	
Receiver Sensitivity (OMAuter),each Lane	SEN			-4.4(For TECQ ≤ 1.8 dB) -6.2 +TECQ (For 1.8 <TECQ ≤ 4.4 dB)	dBm	5
Stressed Receiver Sensitivity(OMAuter), each Lane	SRS			-1.8	dBm	6
LOS Assert	LOSA	-15			dBm	
LOS De-assert				-9.2	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			4.4		dB	
OMAuter of each Aggressor Lane			3.5		dBm	2

Notes:

[1] RMS spectral width is the standard deviation of the spectrum.

[2] If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.

[3] The receiver shall be able to tolerate, without damage,

continuous exposure to a modulated optical input signal having this power level on one lane.

The receiver does not have to operate correctly at this input power.

[4] Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this

value cannot be compliant; however, a value above this does not ensure compliance.

[5] Receiver sensitivity (OMAuter) is informative and is defined for a transmitter with a value of TECQ up to 4.4 dB. Receiver sensitivity should meet Equation (1)

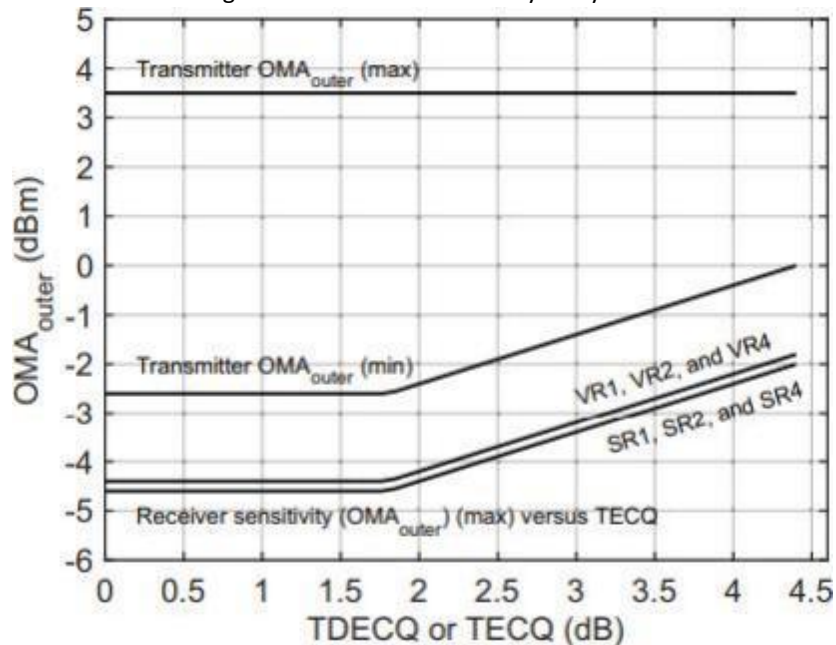
$$RS = \max(-4.4, \text{TECQ} - 6.2) \quad (1)$$

Where: RS is the receiver sensitivity,

and TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.

[6] Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4} .

[7] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



Electrical Characteristics

Parameter	TestPoint	Min.	Typ.	Max.	Unit	Note
Power Consumption				12	W	
Supply Current	Icc			3.83	A	
Module Input (each Lane)						
Data Rate, each Lane	TP1	53.125 ± 100 ppm			GBd	
Differential pk-pk Voltage Tolerance	TP1a	750			mV	
Peak-to-peak AC Common- Mode Voltage	TP1a	3280			mV	
Differential-mode to Common-mode Return	TP1	IEEE			dB	
Effective Return Loss, ERL	TP1	8.5			dB	
Differential Termination Mismatch	TP1			10	%	
Module Stressed Input Tolerance	TP1a	IEEE802.3ck 120G.3.4.3				
Single-ended Voltage Tolerance Range	TP1a	−0.4 to 3.3			V	
DC Common-mode Voltage Tolerance Upper Limit Lower	TP1	2.85 −0.35			V	
Receiver (each Lane)						
Signaling Rate, each Lane	TP4	53.125 ± 100 ppm			GBd	
Peak-to-peak AC Common- mode Voltage Low-frequency, VCMLF Full-band, VCMFB	TP4			32 80	mV	
Differential peak-to-peak Output Voltage Short Mode Long Mode	TP4			600 845	mV	
Eye Height	TP4	15			mV	
Vertical Eye Closure, VEC	TP4			12	dB	

Common-mode to Differential- mode Return loss, RLdc	TP4	IEEE802.3ck Equation (120G-1)			dB	
Effective Return Loss, ERL	TP4	8.5			dB	
Differential Termination Mismatch	TP4	8.5			ps	
DC common-mode Voltage Tolerance Upper Limit Lower Limit	TP4	2.85 -0.35			V	

Digital Diagnostic Monitor Characteristics

Parameter	Symbol	Min.	Max.	Unit	Note
Temperature Monitor Absolute Error	DMI_Temp	-3	3	degC	Over Operating Temperature Range
Supply Voltage Monitor Absolute Error	DMI_VCC	-0.1	0.1	V	Over Full Operating Range
Channel RX Power Monit or Absolute Error	DMI_RX_Ch	-2	2	dB	1
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX Power Monit or Absolute Error	DMI_TX_Ch	-2	2	dB	1

Notes:

- [1] Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Pin Map and Description

The electrical interface of OSFP module consist of a 60 contacts edge connector as illustrated by the diagram in Figure 1, which defined in Clause 8.1 of OSFP MSA Specification.

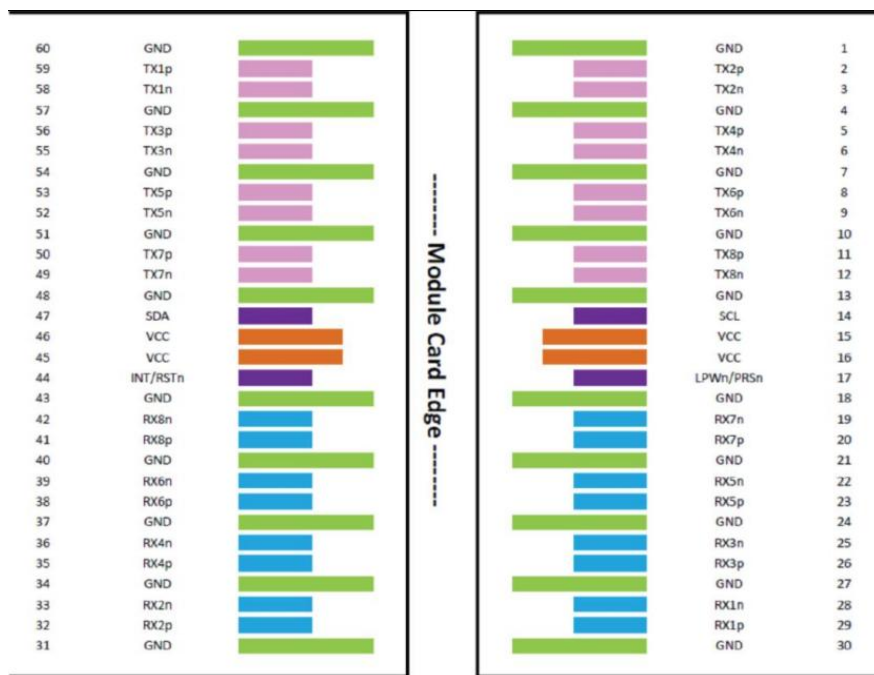


Figure 1. MSA Compliant Connector

Pin#	Symbol	Description	Logic	Direction	Plug
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3

18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

Optical Module Block Diagram

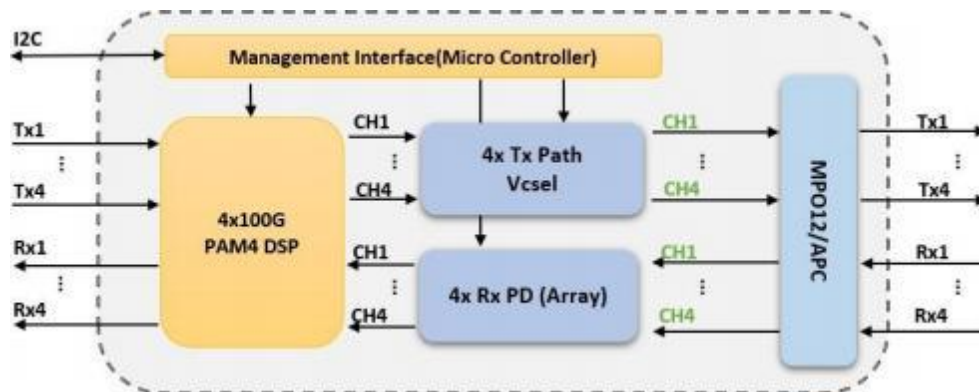


Figure 2. Block Diagram

Recommended Power Supply Filter

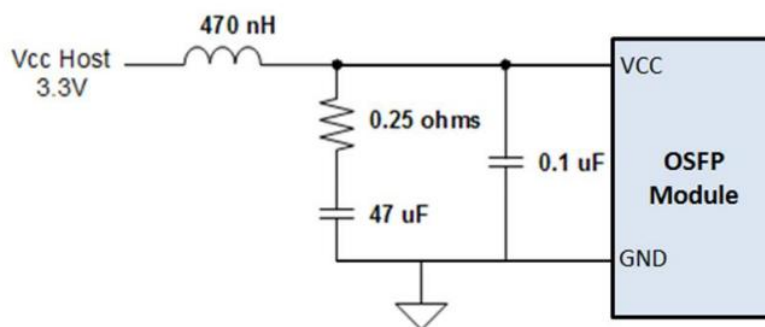


Figure 3. Recommended Power Supply Filter

Optical Interface

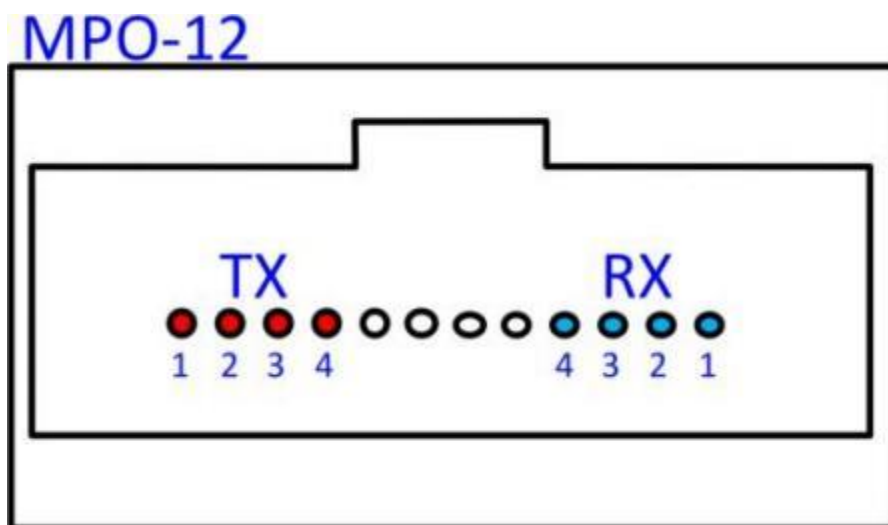


Figure 4. Optical Media Dependent Interface port assignments

Mechanical Drawing

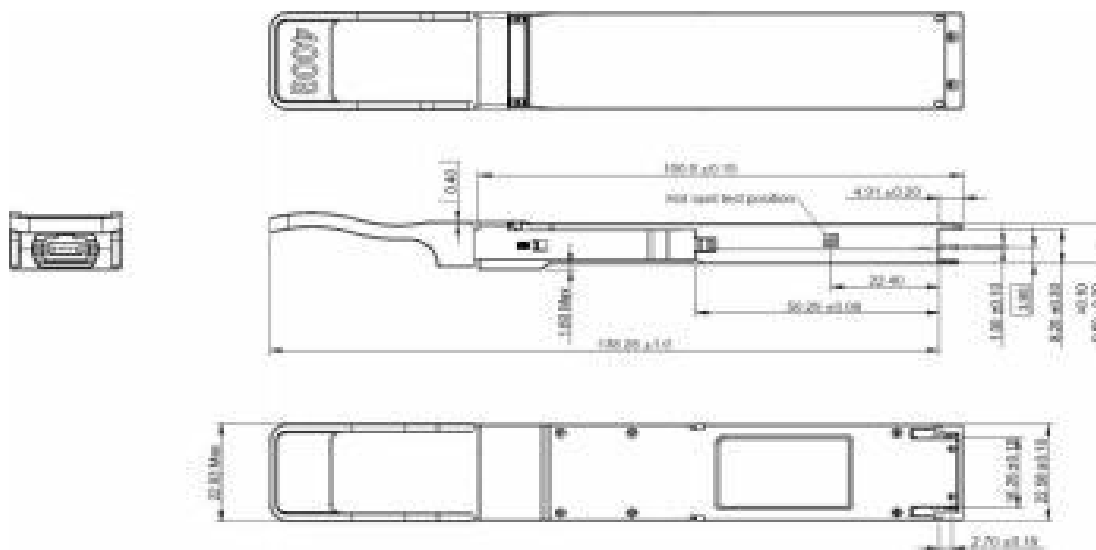


Figure 5. Mechanical Outline

Ordering information

Part Number	Product Description
LO-M85400A-SR4C	OSFP 400G, SR4, MPO-12/APC interface, Flat Top, 850nm, up to 50m, 0° C~+70° C