LO-DM85800B-SR8C

800GBASE-SR8 OSFP 850nm 50m Dual MPO-12/APC Finned Top Transceiver

Features

- Up to 106.25 Gbps Data Rate Per Channel by PAM4 Modulation
- Support 800GAUI-8 Electrical Interface
- Integrated 850nm VCSEL Array and PD Array
- DDM Function Implemented
- Hot-pluggable
- Single +3.3V Power Supply

Applications

- Data Centers and Cloud
- Networks

Standards

- Compliant to OSFP MSA 5.0
- Compliant with CMIS 5.1
- 8x106. 25Gb/s Electrical Interface (800GAUI-8)
- Maximum Power Consumption 16W
- Single +3.3V Power Supply
- Case Temperature Range: 0 ~ +70℃
- RoHS 2.0 Complaint

Description

The LO-DM85800B-SR8C Optical Transceiver Module is designed for use in 800Gb/s systems throughput up to 30m over OM3 or 50m over OM4 multimode fiber (MMF) using a wavelength of 850nm via dual MTP/MPO-12 connectors.

Digital diagnostics functions are also available via the I2C interface, as specified by the OSFP MSA, to allow access to real-time operating parameters. With these features,this easy to install, hot swappable transceiver is suitable to be used in various applications, such as data centers, high-performance computing networks, enterprise core and distribution layer applications.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature Range	TSTG	-40		85	℃	
Supply Voltage	VCC	0		4	V	
Relative Humidity (Non-condensing)	RH	5		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature	Top	0		70	℃	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Consumption	PDISS			16	W	
Pre-FEC Bit Error Ratio				2.4x10-4		
Link Distance with OM4/OM5	D1	2		50	M	
Link Distance with OM3	D2	2		30	M	

Optical Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Wavelength	λ		850		nm	
RMS Spectral Width				0.6	nm	
Modulation Format		PAM4				
Average Launch Power, each Lane	PAVG	-4.6		4	dBm	
Outer Optical Modulation Amplitude(OMAouter), Each Lane						
for TDECQ≤1.8dB		-2.6		3.5	dBm	
for 1.8<TDECQ≤4.4dB		-4.4+TDECQ		3.5	dBm	
Transmitter and Dispersion Eye Closure				4.4	dB	
Transmitter Eye Closure for PAM4 (TECQ),				4.4	dB	
ExtinctionRatio		2.5			dB	
Transmitter Excursion, Each Lane				2	dB	

Transmitter Transition Time, Each Lane				17	ps	
Average Launch Power Per Lane @ TX Off				-30	dBm	
Relative Intensity Noise12 (OMA)				-131	dB/Hz	
Optical Return Loss Tolerance				12	dB	
Encircled Flux		>=86% at 19μm <=30% at 4.5μm			dB	
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Center Wavelength	λ		850		nm	
Damage Threshold, each Lane	THd	5			dBm	
Average Receive Power, each Lane		-6.4		4	dBm	
Receive Power (OMA outer), each Lane				3.5	dBm	
Receiver Sensitivity Each Lane (OMAouter)						
for TECQ≤1.8dB				-4.6	dBm	
for 1.8<TECQ≤4.4dB				-6.4+TECQ	dBm	
Receiver Reflectance				-12	dB	
Stressed Receiver Sensitivity (OMAouter), Each Lane				-2	dBm	
Stressed Conditions for Stress Receiver Sensitivity						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			4.4		dB	
OMAouter of Each Aggressor Lane			3.5		dBm	

High Speed Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Note
Transmitter Electrical Input Characteristics at TP1					
Signaling Rate, Per Lane		53.125		GBd	
Differential Pk-pk Input Voltage Tolerance	900			mV	
Common-mode to Differential Return Loss	802.3ck Equation(120G-1)				
Effective Return Loss	TBD				
Differential Termination Mismatch			10	%	
Module Stressed Input Test	See 120G.3.4.1				
Single-ended Voltage Tolerance Range	-0.4		3.3	V	
DC Common-mode Voltage	350		2850	mV	
Receiver Electrical Output Characteristics at TP4					
Signaling Rate Per Lane		53.125		GBd	
AC common-mode Output Voltage(RMS)			17..5	mV	
Differential Peak-to-peak Output Voltage			900	dB	

Near-end ESMW (Eye Symmetry Mask Width)		-		UI	
Near-end Eyeheight, Differential	24			mV	
Near-end Vertical Eye Closure			7.5	dB	
Far-end ESMW (Eye Symmetry Mask Width)		-		UI	
Far-end Eyeheight, Differential	24			mV	
Far-end Vertical Eye Closure			7.5	dB	
Far-end Pre-cursor ISI Ratio	-			UI	
Common Mode to Differential Conversion Return Loss	802.3ck 120G-1			dB	
Effective Return Loss	TBD			dB	
Differential Termination Mismatch			10	%	
Transition Time (min,20%to80%)		-		ps	
DC Common Mode Voltage	-350		2850	mV	

Low Speed Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit	Note
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for Fast Mode, 20mA for Fast-mode Plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O Pin	Ci		14	pF	
Total Bus Cpacitive Load for SCL and SDA	Cb		100	pF	3.0k Ohms Pull up Resistor, Max
			200	pF	1.6k Ohms Pull up Resistor, Max
LPMode/TxDis, Reset and ModeSelL	VIL	-0.3	0.8	V	|Iin| </= 125uA for Vin < VCC
	VIH	2	Vcc+0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	10k Ohms Pull-up to Host Vcc
Mod PrsL	VOL	0	0.4	%	IOL=2.0mA
	VOH			dB	ModPrsL can be implemented as a short-circuit to GND on the module

Pin Map and Description

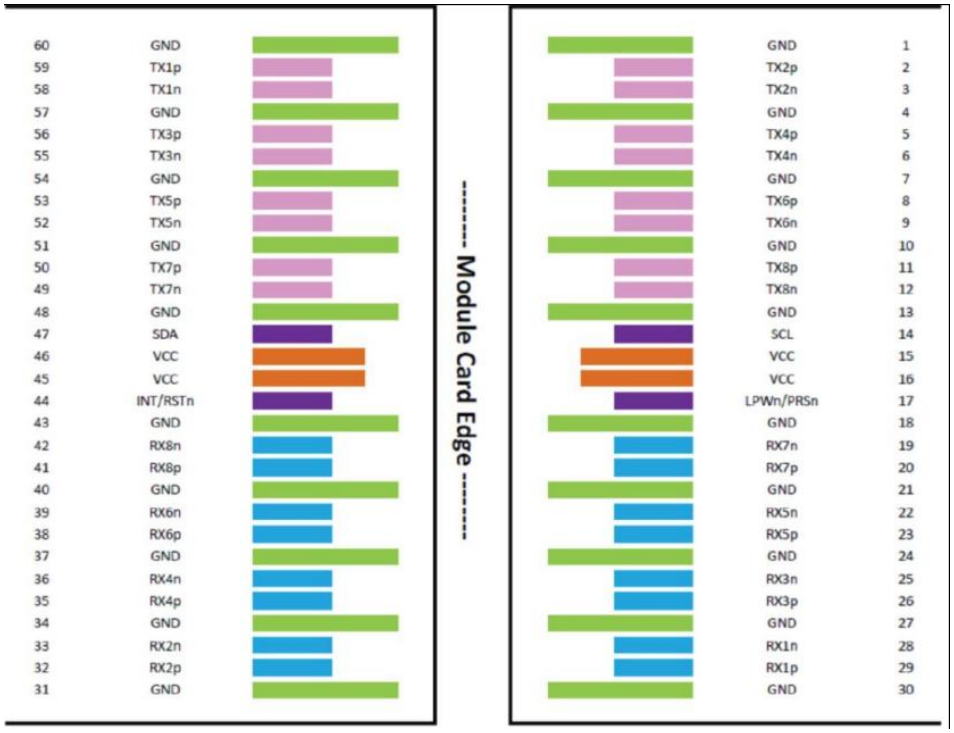

Figure 1. MSA Compliant Connector

Pin#	Symbol	Description	Logic	Direction	Plug
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3

18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

Principle Diagram

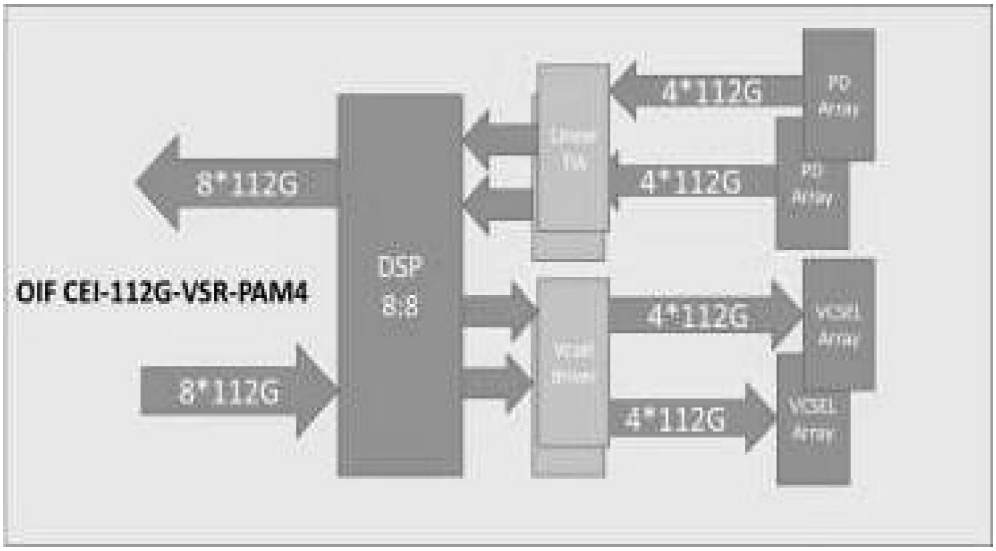

Figure 2.Application Reference Diagram

Mechanical Drawing

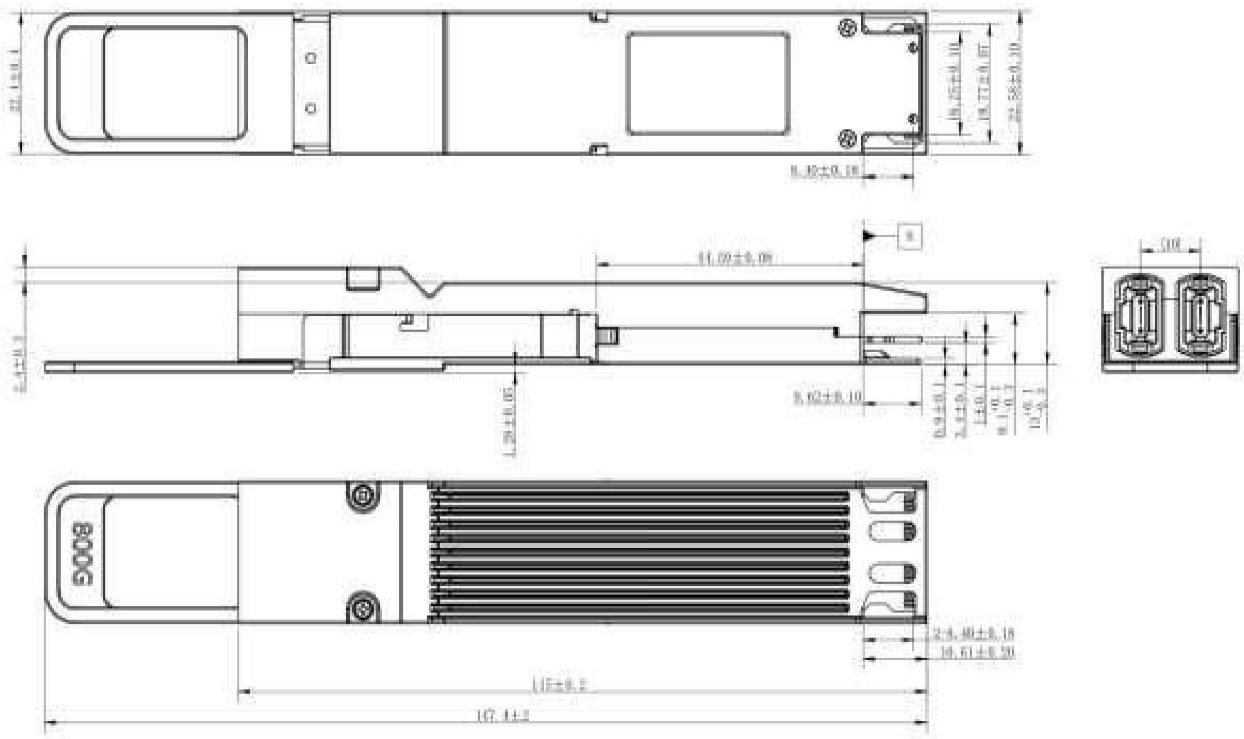

Figure 3. Mechanical Outline

Ordering information

Part Number	Product Description
LO-DM85800B-SR8C	OSFP 800G, SR8, Dual MPO-12/APC interface, Finned Top, 850nm, up to 50m, 0~70°C