LO-DM85800A-SR8C

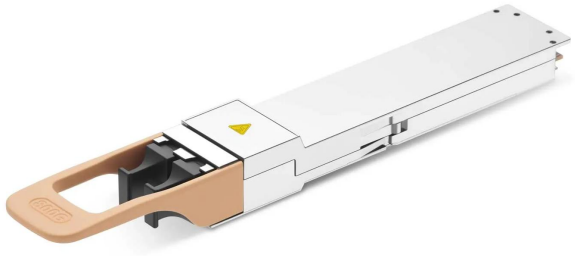
800GBASE-SR8 OSFP 850nm 50m Dual MPO-12/APC FlatTop Transceiver

Features

- Hot-pluggable OSFP form factor
- VCSEL transmitter and PIN PD receiver
- Support 850Gb/s aggregate bit rate
- Support both 8x100G Ethernet and InfiniBand NDR Case
- operating temperature 0°C to 70°C
- Power dissipation < 16W
- Two wire serial Interface with digital diagnostic monitoring
- Class 1 Laser

Applications

- InfiniBand and Ethernet
- Switches, Servers, Routers, Storage Arrays
- Networking Equipment
- Data Centres
- Telecommunication Central Offices
- Test and Measurement Equipment



Standards

- Compliant with CMIS Rev 5.0
- Compliant with IEEE 802.3-2022: 8x100GBASE-VR1 optical interface
- Compliant with IEEE 802.3ck-2022: 8x100GAUI-1 C2M electrical interface
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Compliant with InfiniBand Trade Association (IBTA) Specification 1.6: InfiniBand NDR electrical and optical interface
- Compliant with OSFP MSA Specification Rev 5.0 RHS housing(with the longer body:107.8mm) with Dual MPO- 12/APC receptacle

Description

The OSFP Optical Transceiver is an InfiniBand 800Gb/s 2x400Gb/s Twin-port OSFP, SR8 multimode, parallel, 8-channel transceiver using two, 2-fiber, 4-channel MPO-12/APC optical connectors at 400Gb/s each. The parallel multimode, short reach 8-channel (SR8) uses 100G-PAM4 modulation and has a maximum fiber reach of 50-meters using 8 multimode fibers. It is qualified for use in InfiniBand NDR end-to-end systems.
It is the ideal solution for supercomputing and HPC industries, seamlessly integrating into computing and storage infrastructure to ensure efficient high-performance interconnectivity. The flat-top version is suitable for liquid-cooled and DGX H100/Cedar-7 system links.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature Range	TSTG	-40		85	℃	
Supply Voltage	VCC	-0.5		3.6	V	
Relative Humidity (Non-condensing)	RH	5		85	%	
Data Input Voltage Differential	IVDIP-VDI		1	V	Data	
Control Input Voltage	VI	-0.3		VCC+0.5	V	
Control Output Current	IO	-20		20	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature	TOPR	0		70	ºC	1
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP			6400	mA	
Sustained peak current at hot plug	ICC_SP			5328	mA	
Maximum Power Dissipation	PD			16	W	
Maximum Power Dissipation, Low Power						
Signalling Speed per Lane	DRL		53.125		GBd	
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3		VCC*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)				66	mVpp	
Operating Distance		2		50		1

Notes:1. 0.5m to 30m for OM3, 0.5m to 50m for OM4 and OM5, with FEC.

Optical Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Wavelength	λ	844	850	860	nm	
RMS Spectral Width	RMS			0.65	nm	

Average Launch Power, each Lane	AOPL	-4.6		4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane for max (TECQ, TDECQ) <= 1.8 dB for 1.8 < max (TECQ, TDECQ) <= 4.4 dB	OMAouter	-2.6 -4.4+ max(TECQ, TDECQ)		3.5 3.5	dBm dBm	
Transmitter and Dispersion Eye Closure for PAM4, Each Lane	TDECQ			4.4	dB	
Transmitter Eye Closure for PAM4 (TECQ), Each Lane	TECQ			4.4	dB	
Over/under-shoot				29	%	
ExtinctionRatio	ER	2.5			dB	
Transmitter Excursion, Each Lane				2.3	dB	
Transmitter Transition Time, Each Lane	Tr			17	ps	
Average Launch Power of OFF Transmitter, each lane	TOFF			-30	dBm	
Relative Intensity Noise12 (OMA)	RIN			-132	dB/Hz	
Optical Return Loss Tolerance	ORL			14	dB	
Encircled Flux		>=86% at 19μm <=30% at 4.5μm			dB	
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Center Wavelength	λ	840	850	860	nm	
Damage Threshold, each Lane	THd	5			dBm	
Average Receive Power, each Lane	AOPR	-6.3		4	dBm	
Receive Power (OMA outer), each Lane	OMAR			3.5	dBm	
Receiver Reflectance	RR			-15	dB	
Receiver sensitivity (OMAouter) for TECQ < 1.4 dB for 1.4 dB <=TECQ<=3.4 dB	SOMA			–4.4 –6.2 + TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), Each Lane	SRS			-1.8	dBm	1
Conditions of stressed receiver sensitivity test						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test	SECQ		4.4		dB	
OMAouter of Each Aggressor Lane			3.5		dBm	

High Speed Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Note
Receiver (Module Output, TP4)					
Peak-to-peak AC common-mode voltage					
Low-frequency, VCMLF Full-band, VCMFB			32 80	mV	

Differential peak-to-peak output voltage					
Short mode Long mode			600 845	mV	
Eye height	15			mV	
Vertical eye closure			12	dB	
Common-mode to differential-mode return loss	802.3ck 120G-1			dB	
Effective return loss	8.5			dB	
Differential termination mismatch			10	%	
Transition time	8.5			ps	
DC common-mode voltage tolerance	-0.35		2.85	V	
Transmitter (Module Input, TP1)					
Differential pk-pk input Voltage tolerance (TP1a)	750			mV	
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB	32 80			mV	
Differential-mode to common-mode return loss	802.3ck 120G-2			dB	
Effective return loss	8.5			dB	
Differential termination mismatch			10	%	
Single-ended voltage tolerance range	-0.4		3.3	V	
DC common-mode voltage tolerance	-0.35		2.85	V	

Low Speed Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit	Note
Module output SCL and SDA	VOL	0	0.4	V	
SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
INT/RSTn	Comply with OSFP MSA 5.0 Table 13-4				

Pin Map and Description

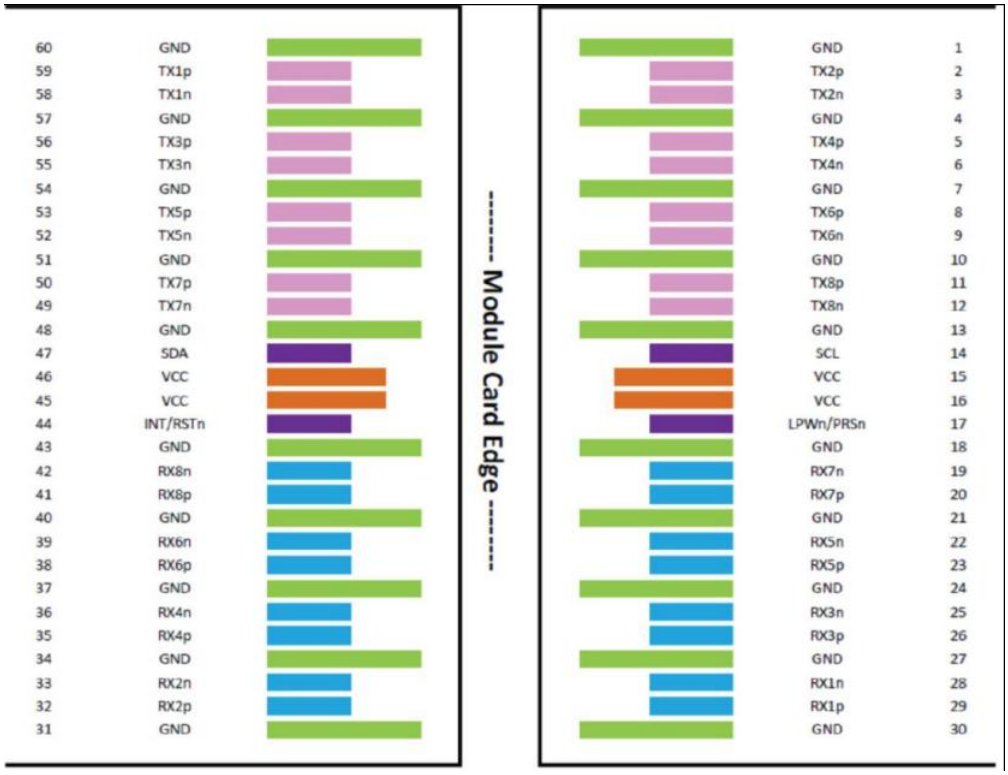


Figure 1. MSA Compliant Connector

Pin#	Symbol	Description	Logic	Direction	Plug
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3

18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

Recommended OSFP Host Board Schematic

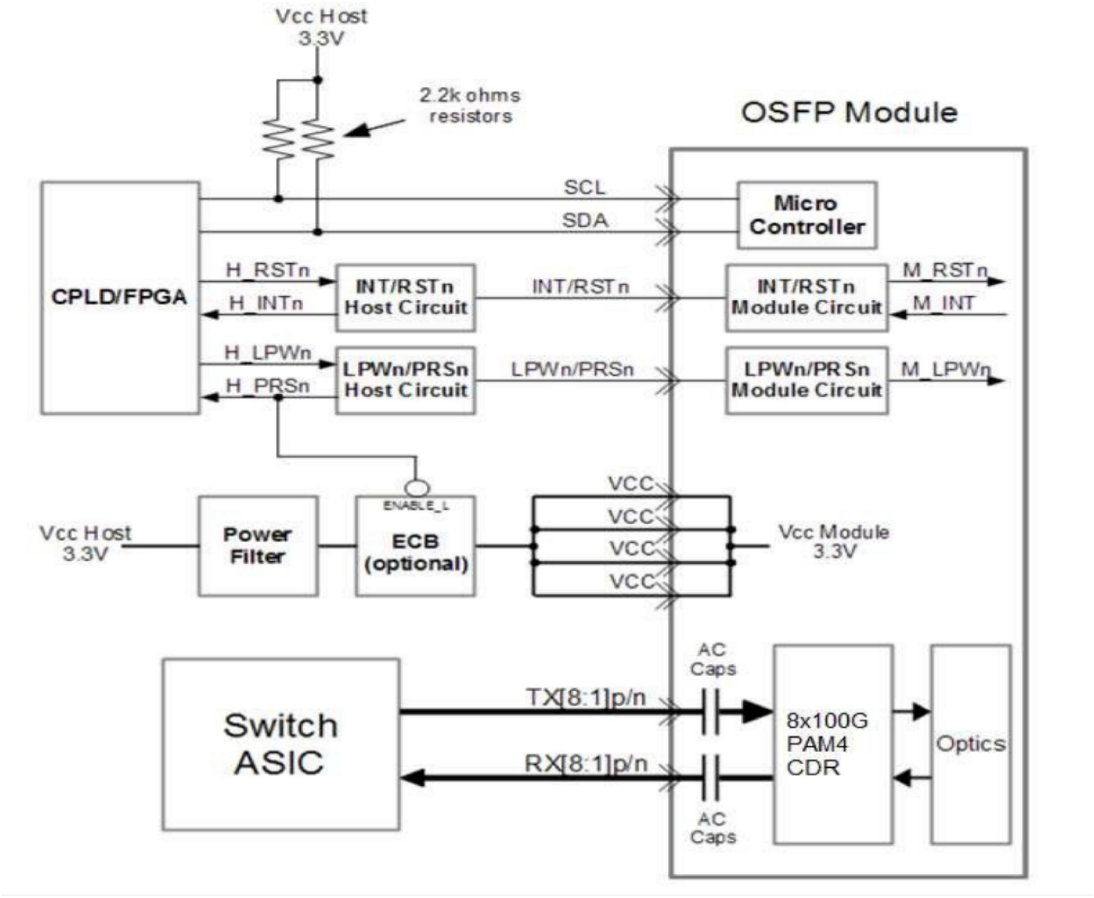


Figure 2. Recommended OSFP Host Board Schematic

Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	3.135 to 3.465	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 15	10%	mA	Internal
Tx Output Power (Each Lane)	-4.6 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-6.3 to +4	±3	dB	Internal

Mechanical Drawing

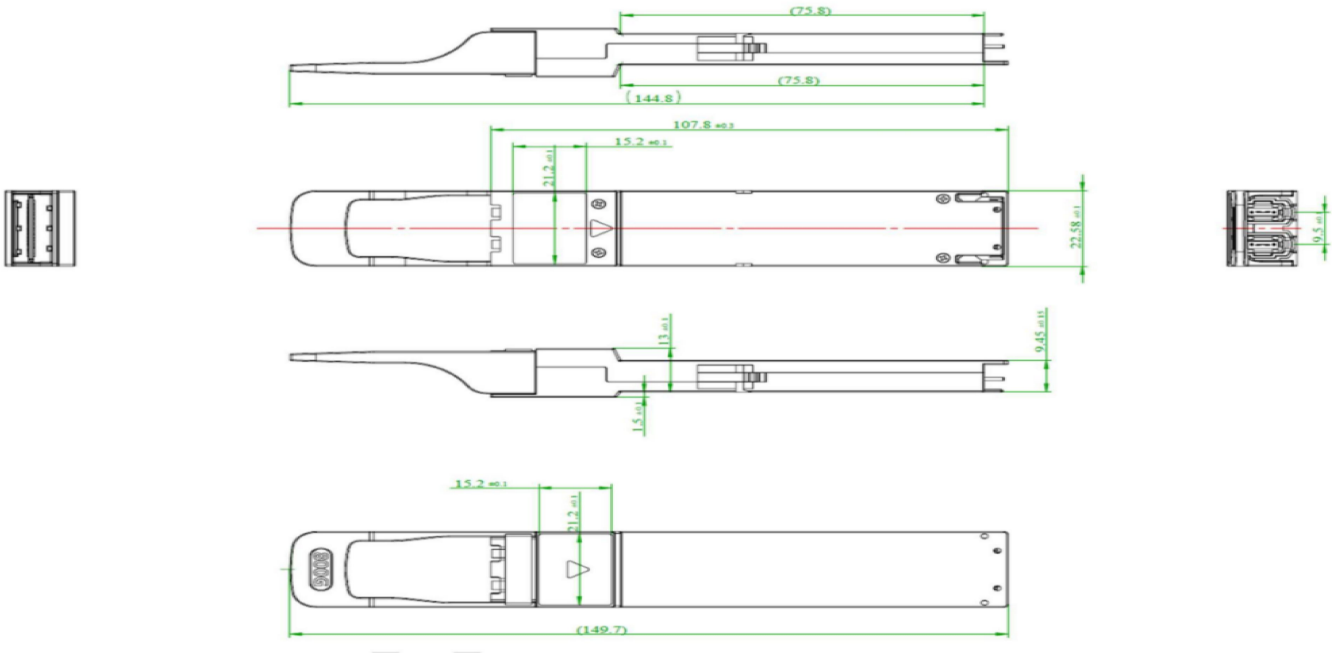


Figure 3. Mechanical Outline

Ordering information

Part Number	Product Description
LO-DM85800A-SR8C	OSFP 800G, SR8, Dual MPO-12/APC interface, FlatTop,PAM4 850nm, 50m, 0~70° C