LO-DM311T-DR8C

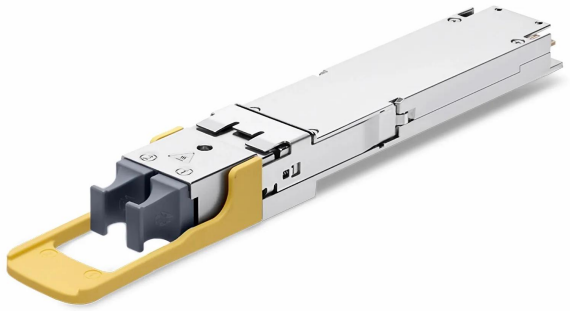
1.6T DR8 OSFP FlatTop 1310nm 500m Dual MPO-12/APC DOM Transceiver

Features

- Hot-pluggable OSFP1600 form factor
- Higher bandwidth EML transmitter and PIN PD receiver
- Support 1.6Tb/s aggregate bit rate
- Support 8x200G Ethernet
- Case operating temperature 0℃ to 70℃
- Class 1 Laser
- Compliant with IEEE802.3dj D1p3:1.6TBASE-DR8 optical interface
- Compliant with IEEE802.3dj D1p3:1.6TAUI-8 C2M electrical interface
- Compliant with OSFP MSA Specification Rev 5.1 RHS type 2 housing with Dual MPO-12/APC receptacle
- Compliant with CMIS Rev 5.3
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Two wire serial Interface with digital diagnostic monitoring

Applications

- 1.6T InifiniBand and Ethernet
- Cloud Networks



Description

The OSFP Optical Transceiver is an1.6T 2x 800Gb/s Twin-port OSFP, 2x DR4/DR8 single mode, parallel, 8-channel transceiver using two, 2- fiber, 4-channel MPO-12/APC optical connectors at 800Gb/s each. The parallel single mode, short reach 8-channel (2x DR4/DR8), uses
200G-PAM4 modulation and has a maximum fiber reach of 500-meters using 8 single mode fibers.
It is the ideal solution for supercomputing and HPC industries, seamlessly integrating into computing and storage infrastructure to ensure efficient high-performance interconnectivity. The flat-top (OSFP-RHS) version is suitable for liquid-cooled switches.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	Ts	-40	85	℃	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	1
Data Input Voltage Differential	lVDIP-VDINl		1	V	
Control Input Voltage	VI	-0.3	VCC+0.5	V	
Control Output Current	IO	-20	20	mA	

Note 1: not to exceed 0.026 kg water/kg of dry air.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Case Temperature	TOPR	0		70	℃	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	ICC_IP			12000	mA	
Sustained Peak Current at Hot Plug	ICC_SP			9990	mA	
Maximum Power Dissipation	PD			30	W	
Maximum Power Dissipation, Low Power Mode	PDLP			2	W	
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3		VCC*0.3	V	
Two Wire Serial Interface Clock Rate				1	MHz	
Voltage Drop Across Mated Connector (Vcc_Host minus Vcc_Module)				66	mVpp	
Operating Distance		2		500	m	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Data Rate, each Lane		106.25 ± 50 ppm			GBd	
Lane Wavelength (range)	λC	1304.5		1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, Each Lane	AOPL	-3.3		4	dBm	2

Outer Optical Modulation Amplitude (OMAouter), Each Lane for Max(TECQ, TDECQ) <0.9 dB for 0.9 dB ≤Max(TECQ, TDECQ) ≤3.4 dB	TOMA	-0.3 – 1.2 + Max(TECQ,TDECQ)		4.2	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), Each Lane	TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4 (TECQ), Each Lane	TECQ			3.4	dB	
| TDECQ – TECQ |				2.5	dB	
Transmitter Overshoot and Undershoot				22	%	
Transmitter Power Excursion				2.3	dBm	
Average Launch Power of OFF Transmitter, Each Lane	TOFF			-15	dBm	
Extinction Ratio, Each Lane	ER	3.5			dB	
Transmitter Transition Time (max)	Tr			8	ps	
RIN21.4OMA (max)	RIN			-139	dB/Hz	
Optical Return Loss Tolerance	ORL			21.4	dB	
Transmitter Reflectance	TR			-26	dB	3
Receiver						
Data Rate, each Lane		106.25 ± 50 ppm			GBd	
Lane Wavelength (range)	λC	1304.5		1317.5	nm	
Damage Threshold, Each Lane	AOPD	5			dBm	
Average Receive Power, Each Lane	AOPR	-6.3		4	dBm	
Receive Power (OMAouter), Each Lane	OMAR			4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMAouter), Each Lane for TECQ < 0.9 dB for 0.9 dB≤ TECQ ≤SECQ	SOMA			-3.4 – 4.3 +TECQ	dBm	1
Stressed Receiver Sensitivity (OMAouter), Each Lane	SRS			-0.9	dBm	1
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test			3.4		dB	
OMAouter of Each Aggressor Lane			4.2		dBm	

Notes:
Note 1: Measured with conformance test signal at TP3 for the BER = 6.4x10-5.
Note 2: Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
Note 3: Transmitter reflectance is defined looking into the transmitter.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Transmitter (Module Input, TP1)						
Signaling Rate, Each Lane (range)		106.25 ± 50 ppm			GBd	
Single-Ended Voltage Tolerance (range)		– 0.4		1.4	V	
DC Common-Mode Voltage Tolerance (range)		– 0.05		1.05	V	
Peak-to-Peak AC Common-Mode Voltage Tolerance						
Low-Frequency, VCMLF		0.032			V	
Full-Band, VCMFB		0.08				
Differential-Mode to Common-Mode Return Loss, RLcd		Equation (179–24)			dB	
Effective Return Loss, ERL		8.5			dB	
Amplitude Tolerance			1		V	
Receiver (Module Output, TP4)						
Signaling Rate, each lane	TP4	106.25 ± 50 ppm			GBd	1
Differential Peak-to-Peak Voltage						
Output Disabled Output Enabled				0.031	V	
DC Common-Mode Voltage Tolerance (range)		– 0.05		1.05	V	
AC Common-Mode Peak-to-Peak Voltage						
Low-Frequency, VCMLF Full-Band, VCMFB				0.015 0.06	V	
Effective Return Loss, ERL		8.5			dB	
Common-Mode to Common-Mode Return Loss, RLcc		Equation (179–16)			dB	
Common-Mode to Differential-Mode Return Loss, RLdc		Equation (179–17)			dB	
Transmitter Steady-State Voltage, vf		0.4		0.5	V	
Linear Fit Pulse Peak Ratio, Rpeak		TBD				
Level Separation Mismatch Ratio RLM		0.95				

Transmitter Output Waveform						
Absolute Value of Step Size for All Taps (min)		0.005				
Absolute Value of Step Size for All Taps (max)		0.025				
Value at Minimum State for c(–3) (max)		-0.06				
Value at Maximum State for c(–2) (min)		0.12				
Value at Minimum State for c(–1) (max)		-0.34				
Value at Minimum State for c(0) (max)		0.5				
Value at Minimum State for c(1) (max)		-0.2				
Difference Signal-to-Noise-and-Distortion Ratio,DSNDR		0			dB	
Signal-to-Residual-Intersymbol-InterferenceRatio,SNRISI		28			dB	
Output Jitter						
JRMS03 EOJ03				0.023 0.025	UI	
J4u03				0.118		

Note 1: The signaling rate is derived from the PMD receiver input.

Electrical Characteristics Low Speed Signal

Parameter	Symbol	Min.	Max.	Unit	Condition
Module Output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
INT/RSTn		Comply with OSFP MSA 5.1 Table 14-4			

Pin Map and Description

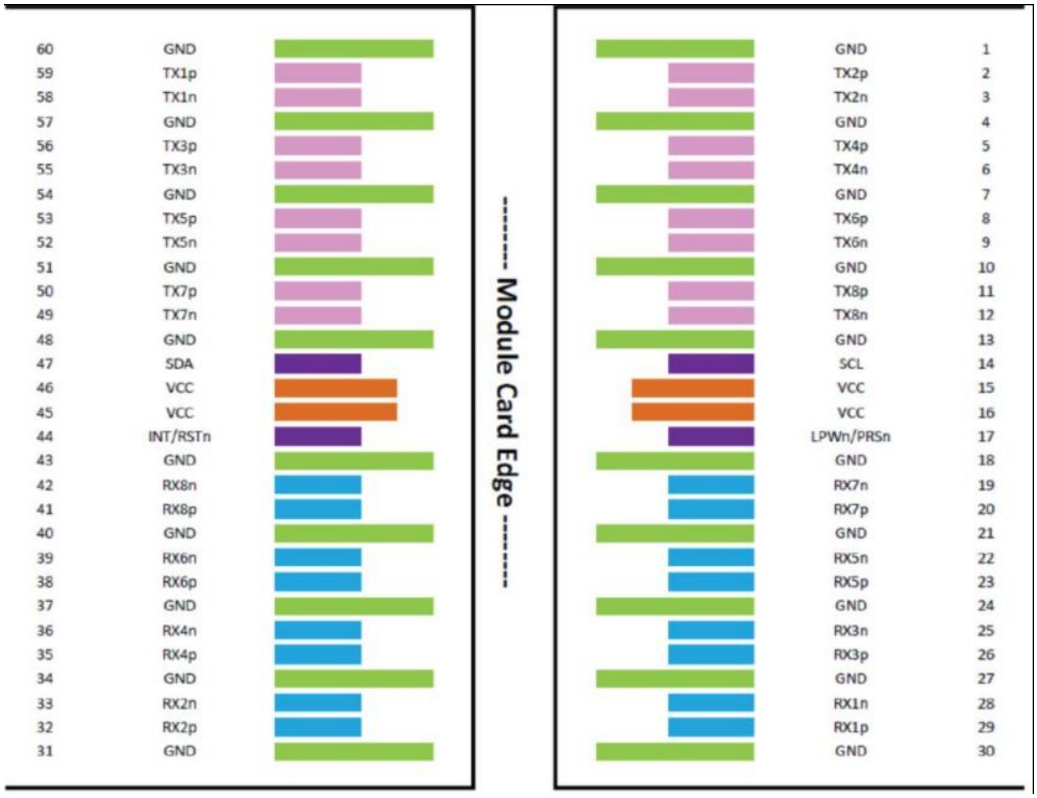


Figure 1. MSA Compliant Connector

Pin#	Symbol	Description	Logic	Direction	Plug
1	GND		Ground		1
2	TX2p	Transmitter	CML-I	Input from Host	3
3	TX2n	Transmitter	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter	CML-I	Input from Host	3
6	TX4n	Transmitter	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter	CML-I	Input from Host	3
9	TX6n	Transmitter	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter	CML-I	Input from Host	3
12	TX8n	Transmitter	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power	Multi-Level	Bi-directional	3

18	GND		Ground		1
19	RX7n	Receiver Data	CML-O	Output to Host	3
20	RX7p	Receiver Data	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data	CML-O	Output to Host	3
23	RX5p	Receiver Data	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data	CML-O	Output to Host	3
26	RX3p	Receiver Data	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data	CML-O	Output to Host	3
29	RX1p	Receiver Data	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data	CML-O	Output to Host	3
33	RX2n	Receiver Data	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data	CML-O	Output to Host	3
36	RX4n	Receiver Data	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data	CML-O	Output to Host	3
39	RX6n	Receiver Data	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data	CML-O	Output to Host	3
42	RX8n	Receiver Data	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter	CML-I	Input from Host	3
50	TX7p	Transmitter	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter	CML-I	Input from Host	3
53	TX5p	Transmitter	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter	CML-I	Input from Host	3
56	TX3p	Transmitter	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter	CML-I	Input from Host	3
59	TX1p	Transmitter	CML-I	Input from Host	3
60	GND		Ground		1

OSFP Control pins

Name	Direction	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	Input/Output	Dual Function Signal . Low Power mode is an active-low input signal . Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal Voltage zones is shown as figure3.
INT/RSTn	Input/Output	Dual Funtion Signal . Reset is an active-low input signal . Interrupt is an active-high output signal Voltage zones is shown as figure 3.

Electrical Characteristics Low Speed Signal

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	℃	Internal
Voltage	3.135 to 3.465	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 120	10%	mA	Internal
Tx Output Power (Each Lane)	-3.3 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-6.3 to +4	±3	dB	Internal

Recommended OSFP Host Board Schematic

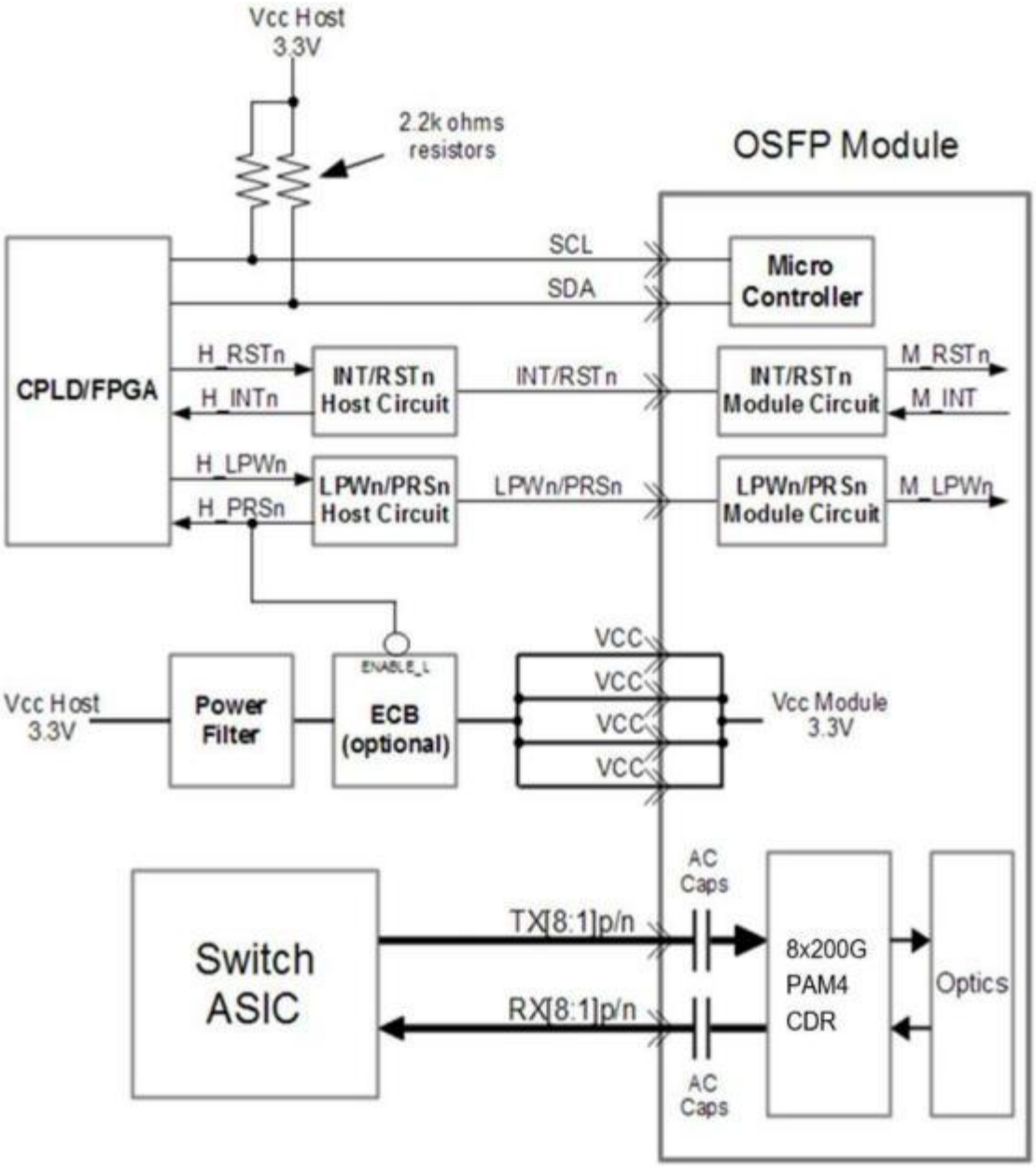


Figure 2. Host Board Schematic

Mechanical Drawing

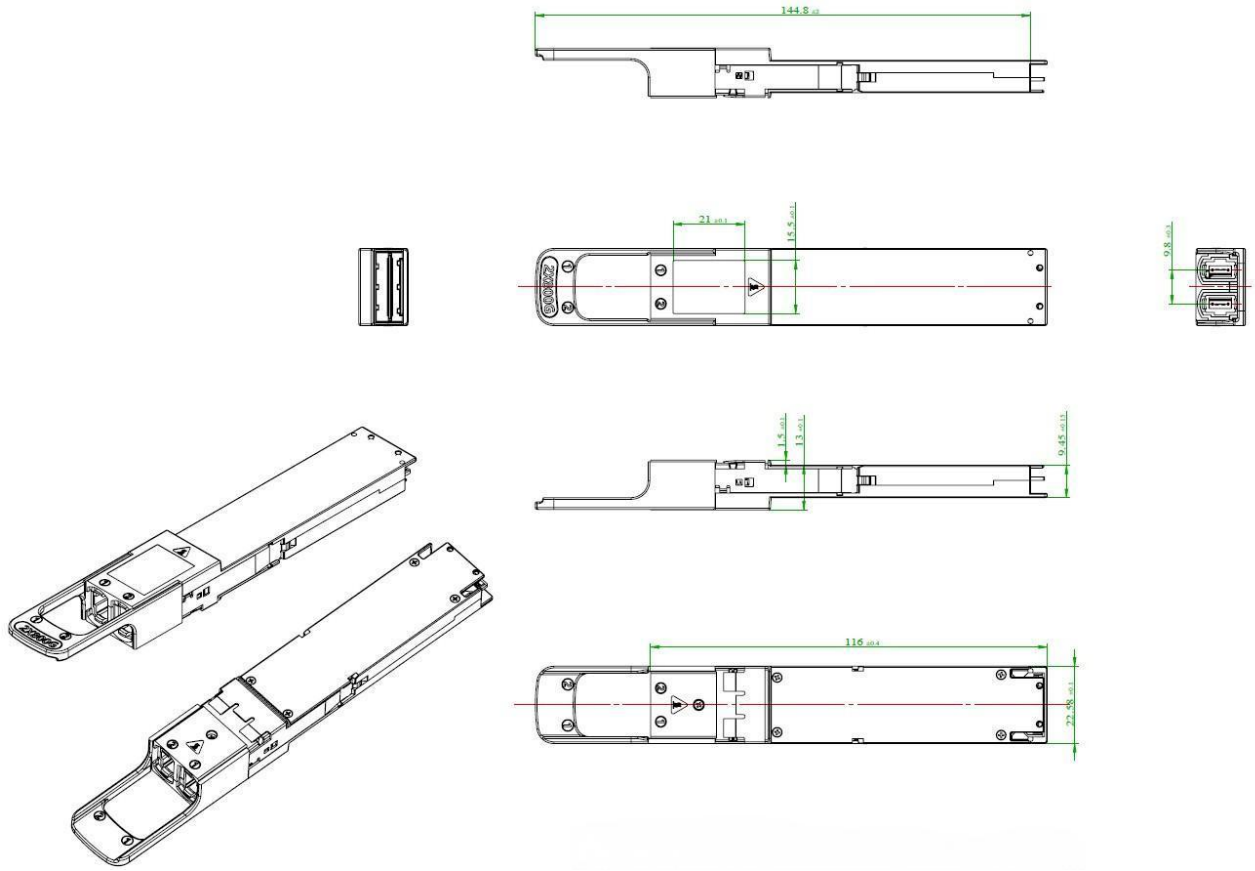


Figure 3. Mechanical Outline

Ordering information

Part Number	Product Description
LO-DM311T-DR8C	OSFP,Dual MPO-12/APC, 1310nm, 1.6T, DR8, 0~70℃, Flat Top, DOM Transceiver